NuMicro™ NUC230/240 Series Product Brief

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TABLE OF CONTENTS

List of Figures

List of Tables

1 GENERAL DESCRIPTION

The NuMicro™ NUC230 CAN Line is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer (WDT), Window Watchdog Timer (WWDT), RTC, PDMA with CRC calculation unit, UART, SPI, I^2C, I^2S, PWM, GPIO, LIN, CAN, PS/2, ISO-7816-3 (Smart Card Host), 800 kSPS high speed 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

The NuMicro™ NUC240 Connectivity Line with USB 2.0 FS and CAN function is embedded with the Cortex™-M0 core running up to 72 MHz and features 32K/64K/128K bytes flash, 8K/16K bytes SRAM, and 8 Kbytes loader ROM for the ISP. It is also equipped with plenty of peripheral devices, such as Timers, Watchdog Timer (WDT), Window Watchdog Timer (WWDT), RTC, PDMA with CRC calculation unit, UART, SPI, I^2C, I^2S, PWM, GPIO, LIN, CAN, PS/2, USB 2.0 FS Device, ISO-7816-3 (Smart Card Host), 800 kSPS high speed 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I^2C	USB	LIN	CAN	PS/2	I^2S	ISO-7816
NUC230	•	•	•		•	•	•	•	•
NUC240	•	•	•	•	•	•	•	•	•

Table 1-1 NuMicro™ NUC230/240 Series Connectivity Support Table

2 FEATURES

- ARM® Cortex™-M0 core
  - Runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K/128K bytes Flash for program code
  - 8 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Configurable data flash address and size for 128 KB system, fixed 4 KB data flash for the 32 KB and 64 KB system
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM
  - 8K/16K bytes SRAM
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 9 channels PDMA for automatic data transfer between SRAM and peripherals
  - Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25℃ and V_{DD} = 5 V
    - Trimmed to ±3 % at -40℃ ~ +105℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 72 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting

- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- WDT
  - Multiple clock sources
    - System clock (HCLK)
    - External 32 kHz crystal (LXT)
    - Internal 10 kHz oscillator (LIRC)
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- WWDT
  - 6-bit down counter with 11-bit prescale for wide range window selected
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports battery power pin (V_{BAT})
  - Supports wake-up function
- PWM/Capture
  - Up to four built-in 16-bit PWM generators providing eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital capture timers (shared with PWM timers) providing eight rising/falling capture inputs
  - Supports PWM trigger ADC to conversion in Center-aligned type
  - Supports Capture interrupt
- UART
  - Up to six UART controllers (three UART controllers are shared with ISO-7816-3 UART mode)
  - UART ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0 with 64-byte FIFO is for 1 Mbps high speed
  - UART1 and UART2 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports PDMA mode

- ISO-7816-3 (Smart Card Host, SC)
  - Supports up to three ISO-7816-3 ports
    - Compliant to ISO-7816-3 T=0, T=1
    - Separate receive / transmit 4 bytes entry FIFO for data payloads
    - Programmable transmission clock frequency
    - Programmable receiver buffer trigger level
    - Programmable guard time selection (11 ETU ~ 266 ETU)
    - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
    - Supports auto inverse convention function
    - Supports transmitter and receiver error retry and error limit function
    - Supports hardware activation/warm reset/deactivation sequence process
    - Supports hardware auto deactivation sequence when detecting the card is removal
  - Supports up to three UART ports
    - Full duplex, asynchronous communications
    - Supports receiving / transmitting 4-bytes FIFO
    - Supports programmable baud rate generator for each channel
    - Programmable even, odd or no parity bit generation and detection
    - Programmable stop bit, 1 or 2 stop bit generation
- SPI
  - Up to four sets of SPI controllers
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and one slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
  - Supports PDMA mode
  - Supports three wired, no slave select signal, bi-directional interface
- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allowing for versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports wake-up function

- I^2S
  - Interface with external audio CODEC
  - Operates as either Master or Slave mode
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - Software override bus
- CAN 2.0
  - Support two sets of CAN devices
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1 Mbps
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Supports power down wake-up function
- USB 2.0 Full-Speed Device (NUC240 series only)
  - One set of USB 2.0 FS Device (12 Mbps)
  - On-chip USB Transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Includes 512 Bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
- ADC
  - 12-bit SAR ADC with 800 kSPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion started by software programming or external input
  - Supports PDMA mode
- Analog Comparator
  - Up to two analog comparators
  - External input or internal Band-gap voltage selectable at negative node
  - Interrupt when compare result change
  - Supports Power-down wake-up

- 96-bit unique ID (UID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out Detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage level: 2.0 V
- Operating Temperature: -40℃ ~ +105℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC230/240xxxAE Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-bit)	Connectivity						ISO-7816-3 **	I²S	PWM (16-bit)	ADC (12-bit)	Comparator	RTC	ISP/ICP/IAP	Package
							UART *	SPI	I²C	USB	LIN	CAN								
NUC230 CAN Line																				
NUC230LC2AE	32	8	4	8	35	4	3+2	1	2	--	3	2	2	1	4	7	1	√	√	LQFP48
NUC230LD2AE	64	8	4	8	35	4	3+2	1	2	--	3	2	2	1	4	7	1	√	√	LQFP48
NUC230LE3AE	128	16	Config.	8	35	4	3+2	1	2	--	3	2	2	1	4	7	1	√	√	LQFP48
NUC230SC2AE	32	8	4	8	49	4	3+2	2	2	--	3	2	2	1	6	7	2	√	√	LQFP64
NUC230SD2AE	64	8	4	8	49	4	3+2	2	2	--	3	2	2	1	6	7	2	√	√	LQFP64
NUC230SE3AE	128	16	Config.	8	49	4	3+2	2	2	--	3	2	2	1	6	7	2	√	√	LQFP64
NUC230VE3AE	128	16	Config.	8	83	4	3+3	4	2	--	3	2	3	1	8	8	2	√	√	LQFP100
NUC240 Connectivity Line																				
NUC240LC2AE	32	8	4	8	31	4	3+1	1	2	1	2	2	1	1	4	7	1	√	√	LQFP48
NUC240LD2AE	64	8	4	8	31	4	3+1	1	2	1	2	2	1	1	4	7	1	√	√	LQFP48
NUC240LE3AE	128	16	Config.	8	31	4	3+1	1	2	1	2	2	1	1	4	7	1	√	√	LQFP48
NUC240SC2AE	32	8	4	8	45	4	3+2	2	2	1	3	2	2	1	4	7	2	√	√	LQFP64
NUC240SD2AE	64	8	4	8	45	4	3+2	2	2	1	3	2	2	1	4	7	2	√	√	LQFP64
NUC240SE3AE	128	16	Config.	8	45	4	3+2	2	2	1	3	2	2	1	4	7	2	√	√	LQFP64
NUC240VE3AE	128	16	Config.	8	79	4	3+3	4	2	1	3	2	3	1	8	8	2	√	√	LQFP100

Note:

*: Marked in the table (3+1) means 3 UART+ 1 ISO-7816 UART function.

**: ISO-7816 UART supports full duplex mode.

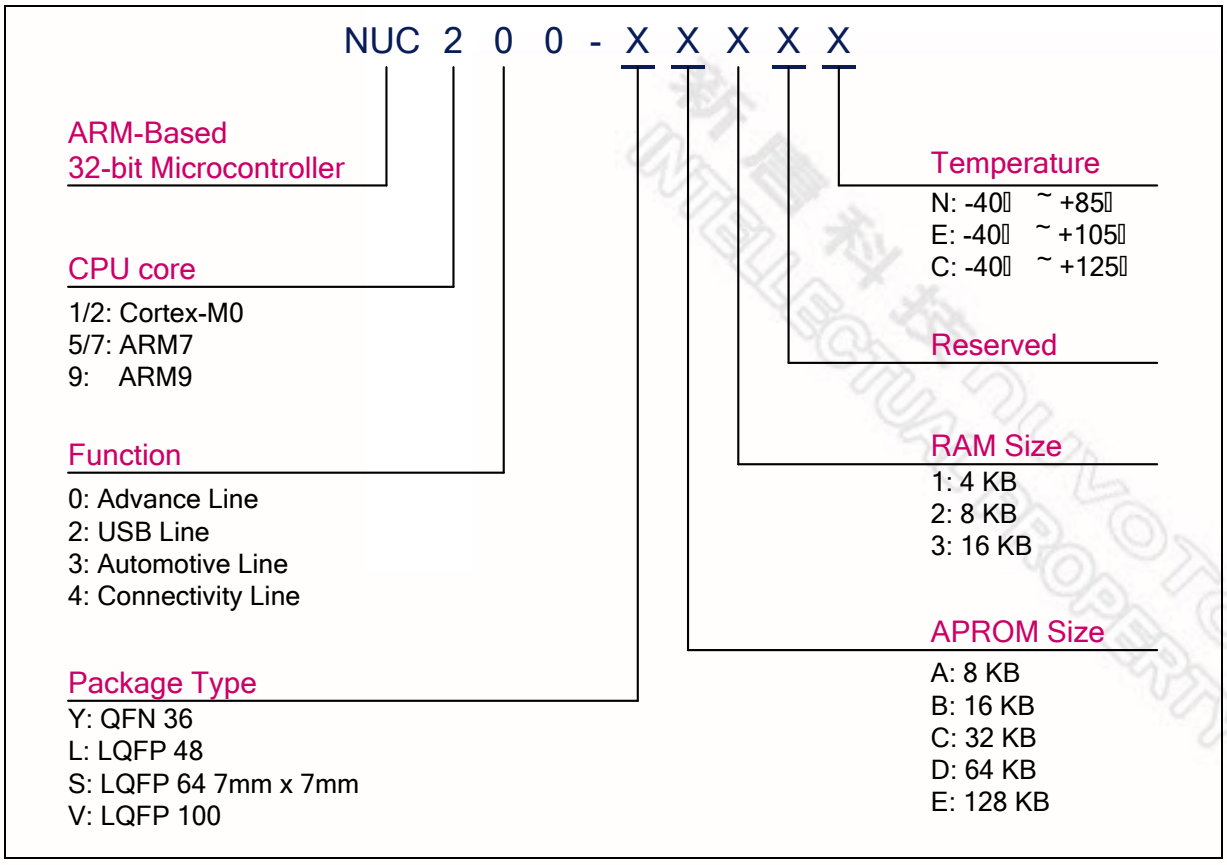


Figure 3-1 NuMicro™ NUC230/240 Series Selection Code

3.2 Pin Configuration

3.2.1 NuMicro™ NUC230 Pin Diagram

3.2.1.1 *NuMicro™ NUC230VxxAE LQFP 100 pin*

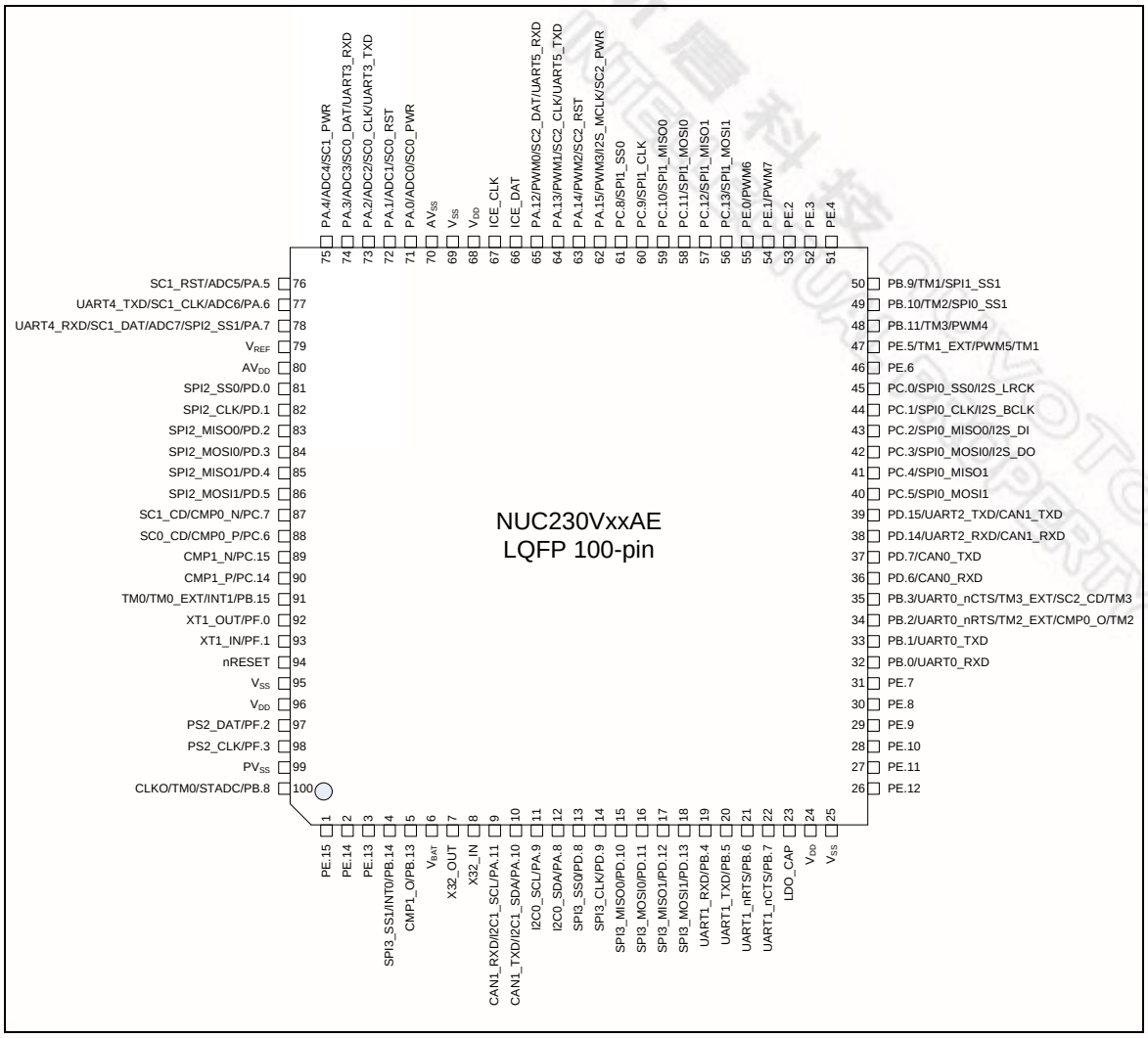


Figure 3-2 NuMicro™ NUC230VxxAE LQFP 100-pin Diagram

3.2.1.2 *NuMicro™ NUC230SxxAE LQFP 64 pin*

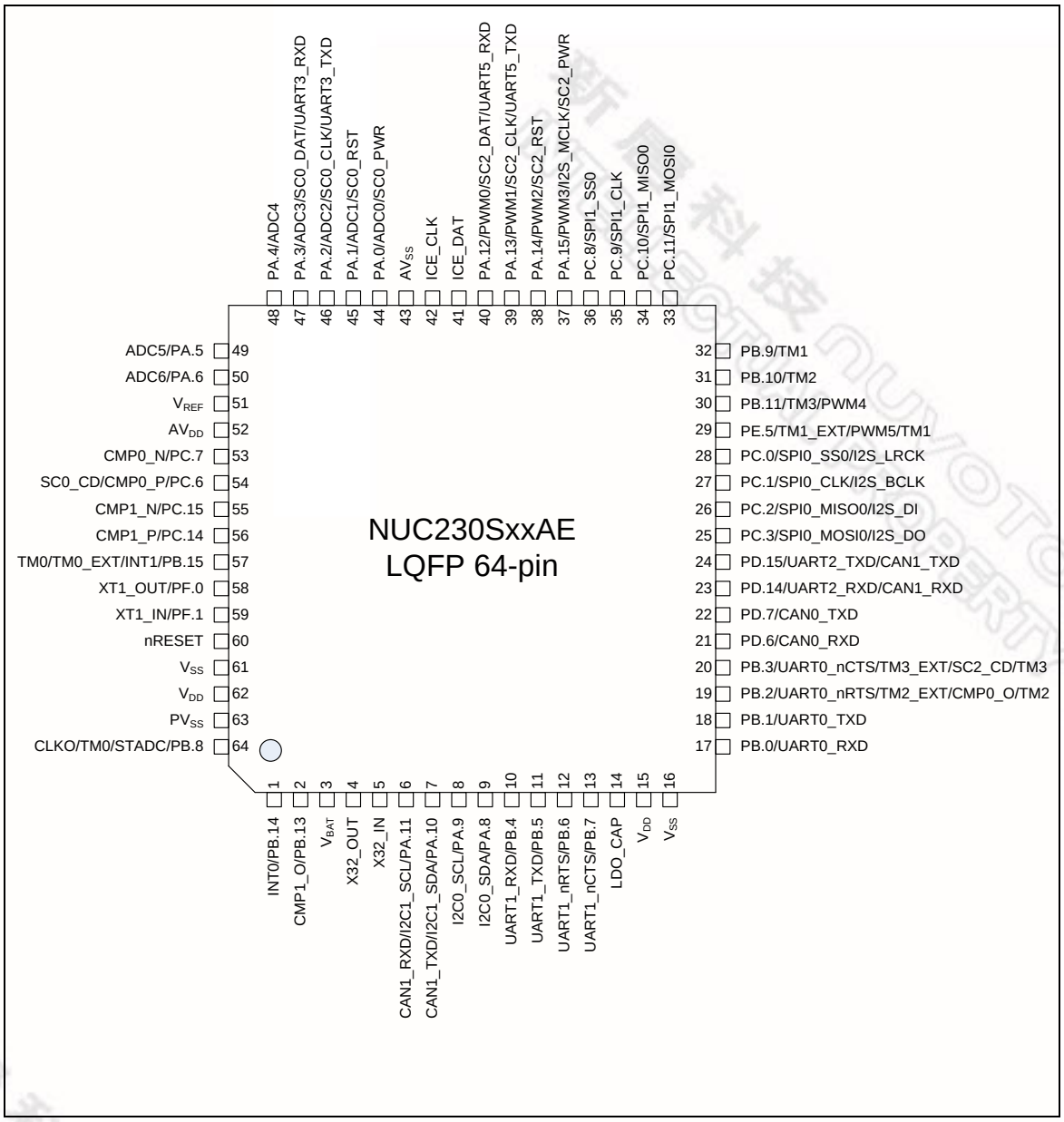


Figure 3-3 NuMicro™ NUC230SxxAE LQFP 64-pin Diagram

3.2.1.3 *NuMicro™ NUC230LxxAE LQFP 48 pin*

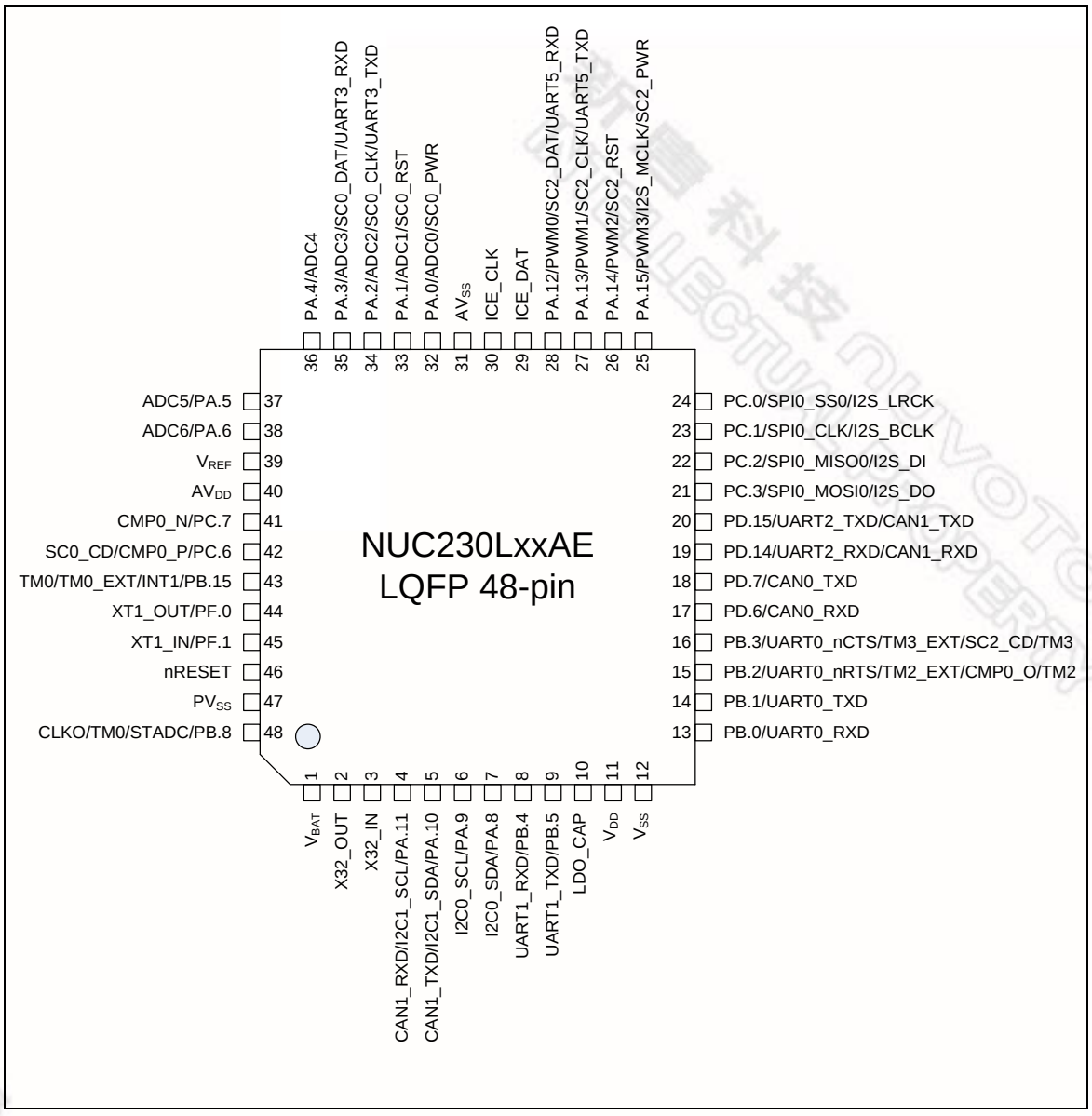


Figure 3-4 NuMicro™ NUC230LxxAE LQFP 48-pin Diagram

3.2.2 NuMicro™ NUC240 Pin Diagram

3.2.2.1 *NuMicro™ NUC240VxxAE LQFP 100 pin*

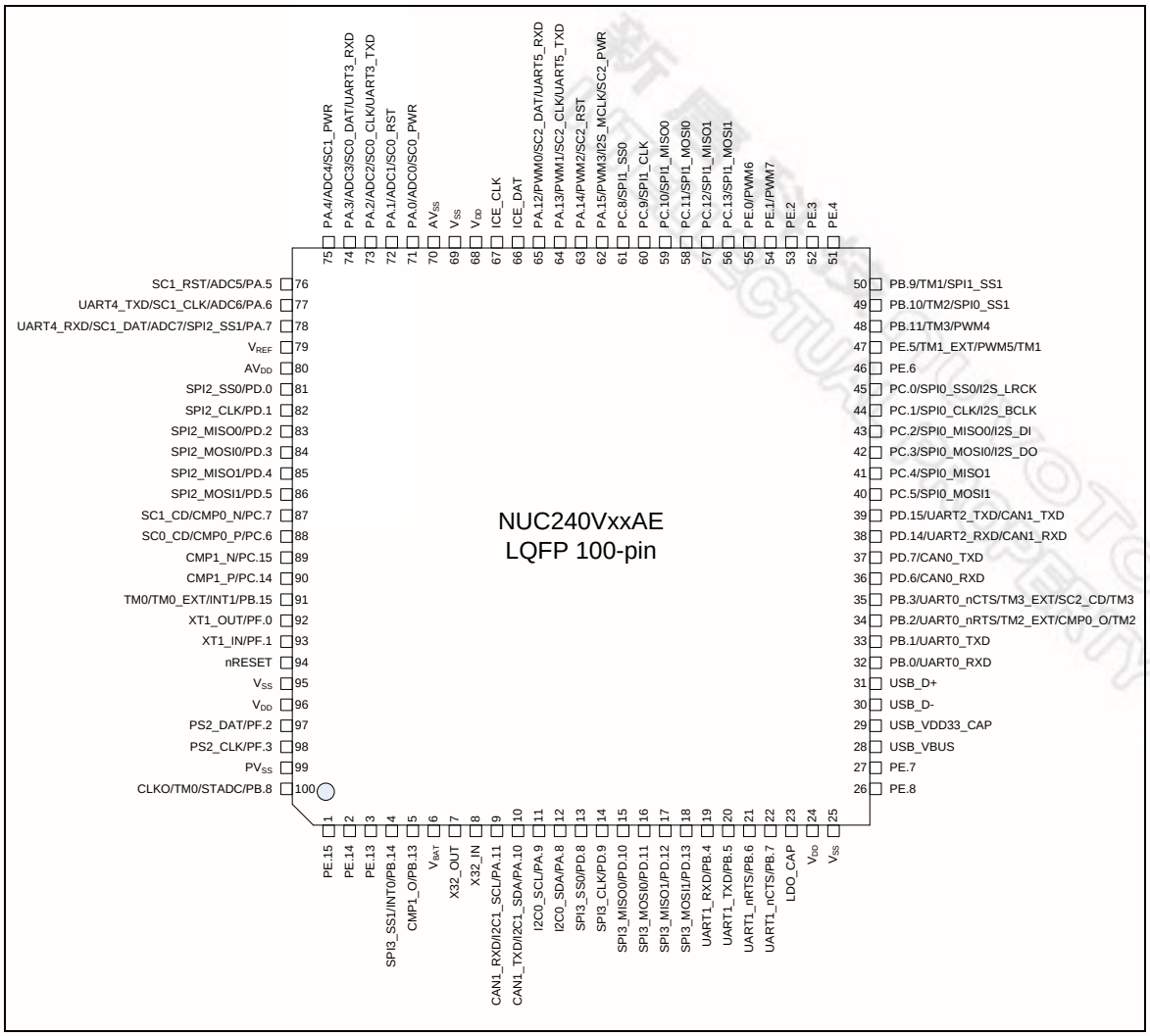


Figure 3-5 NuMicro™ NUC240VxxAE LQFP 100-pin Diagram

3.2.2.2 *NuMicro™ NUC240SxxAE LQFP 64 pin*

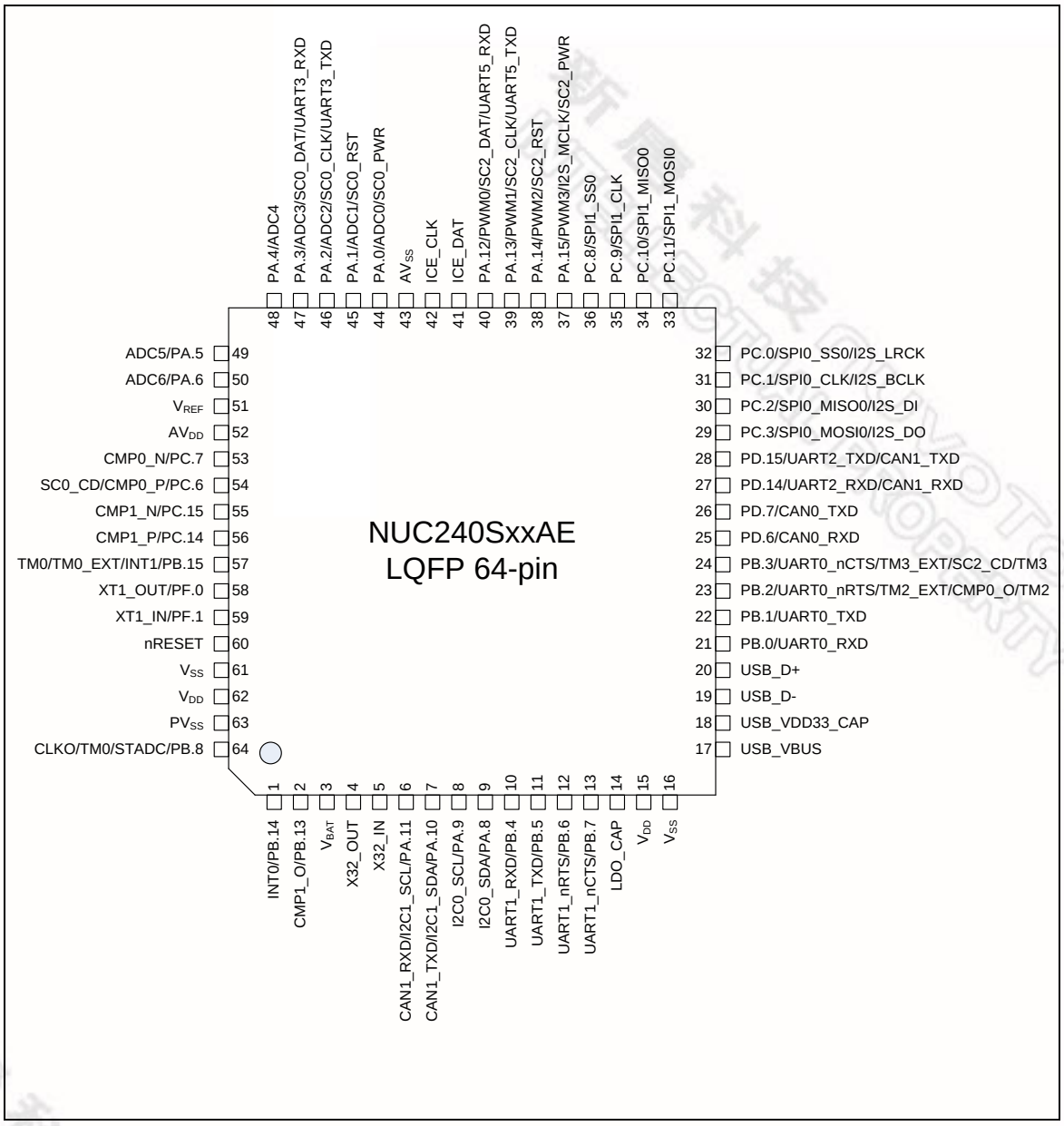


Figure 3-6 NuMicro™ NUC240SxxAE LQFP 64-pin Diagram

3.2.2.3 *NuMicro™ NUC240LxxAE LQFP 48 pin*

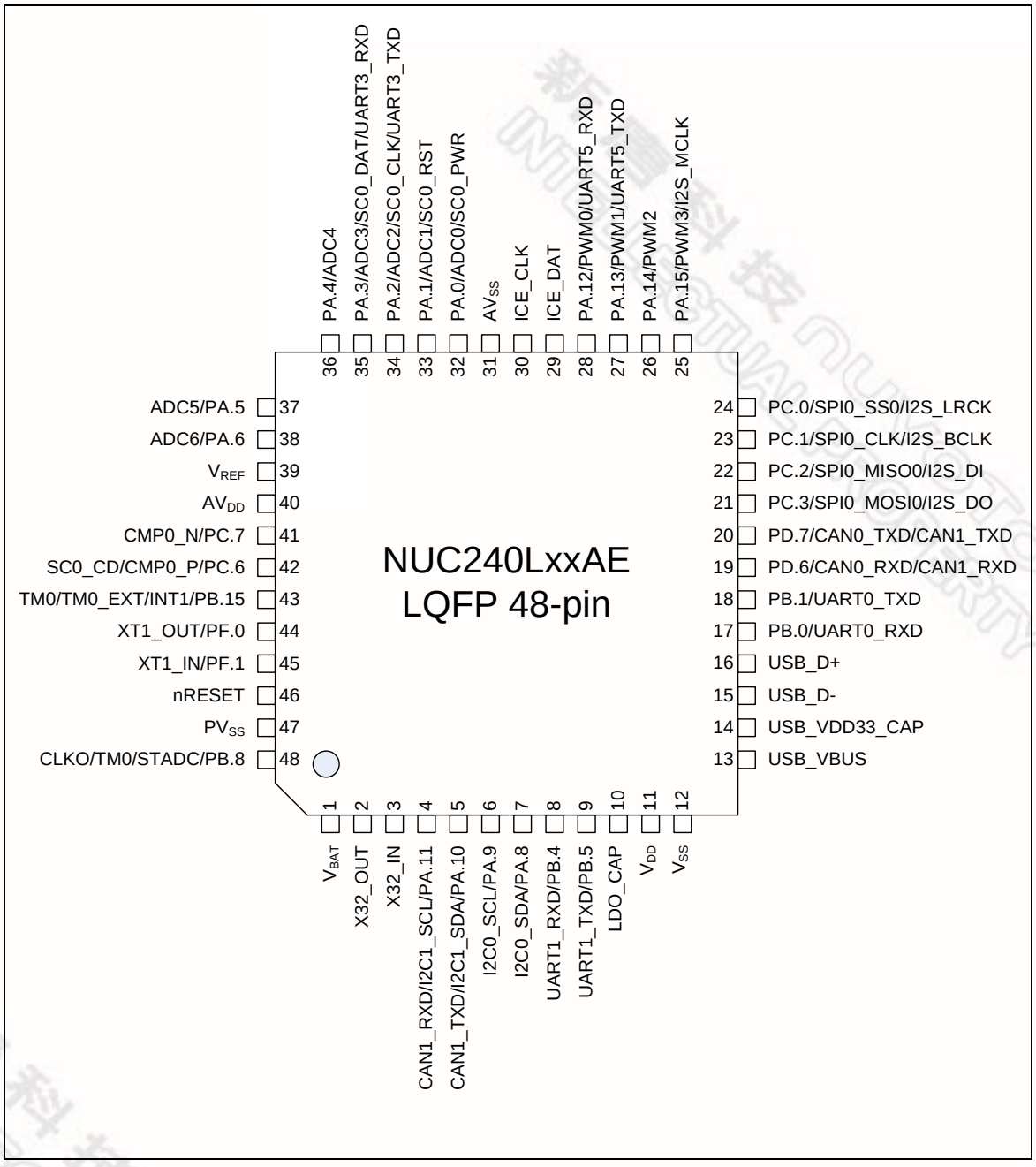


Figure 3-7 NuMicro™ NUC240LxxAE LQFP 48-pin Diagram

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC230/240 Block Diagram

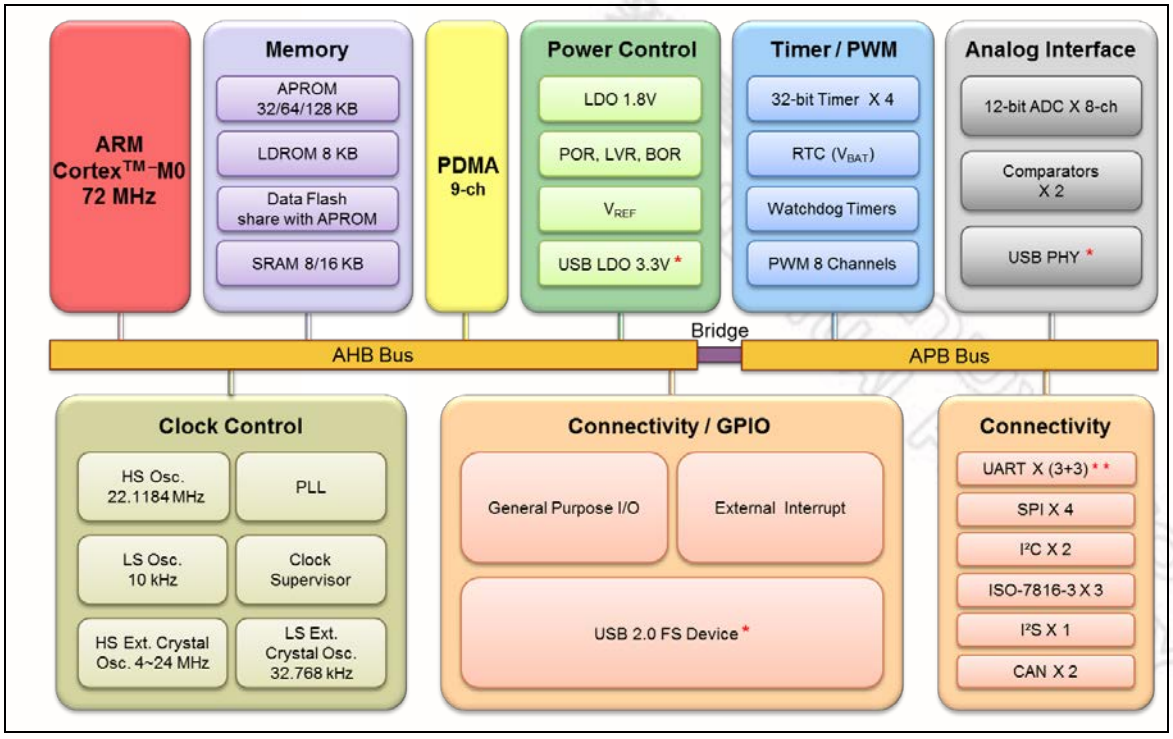


Figure 4-1 NuMicro™ NUC230/240 Block Diagram

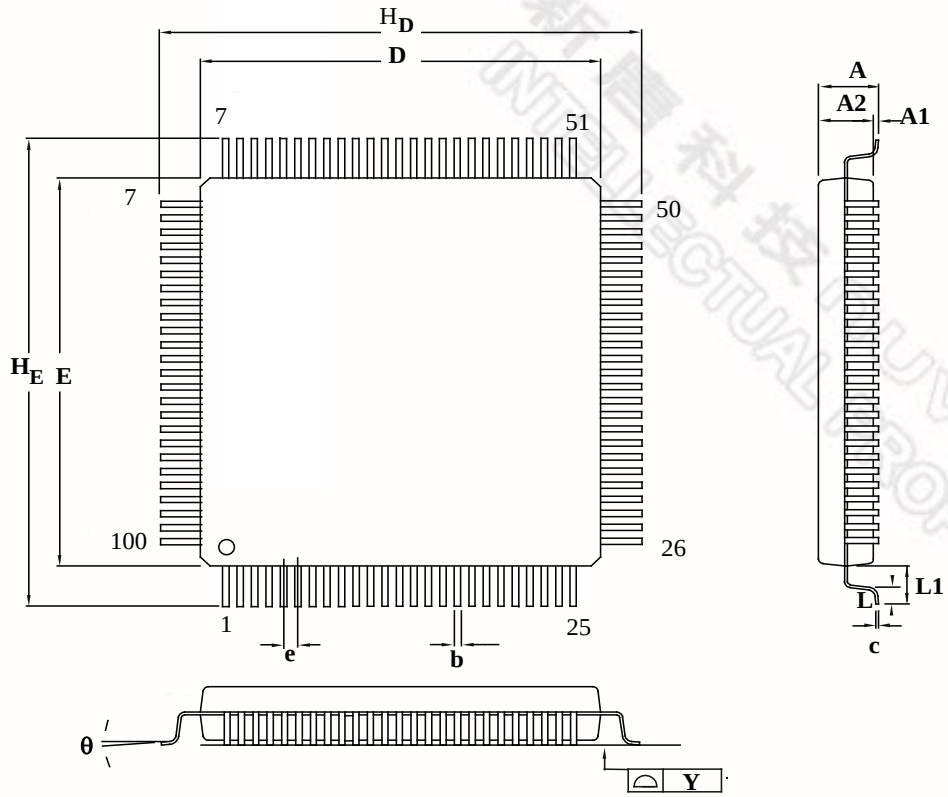
Note:

*: NUC240 only.

**: Marked UART in the table (3+3) means 3 UART+ 3 ISO-7816 UART function.

5 PACKAGE DIMENSIONS

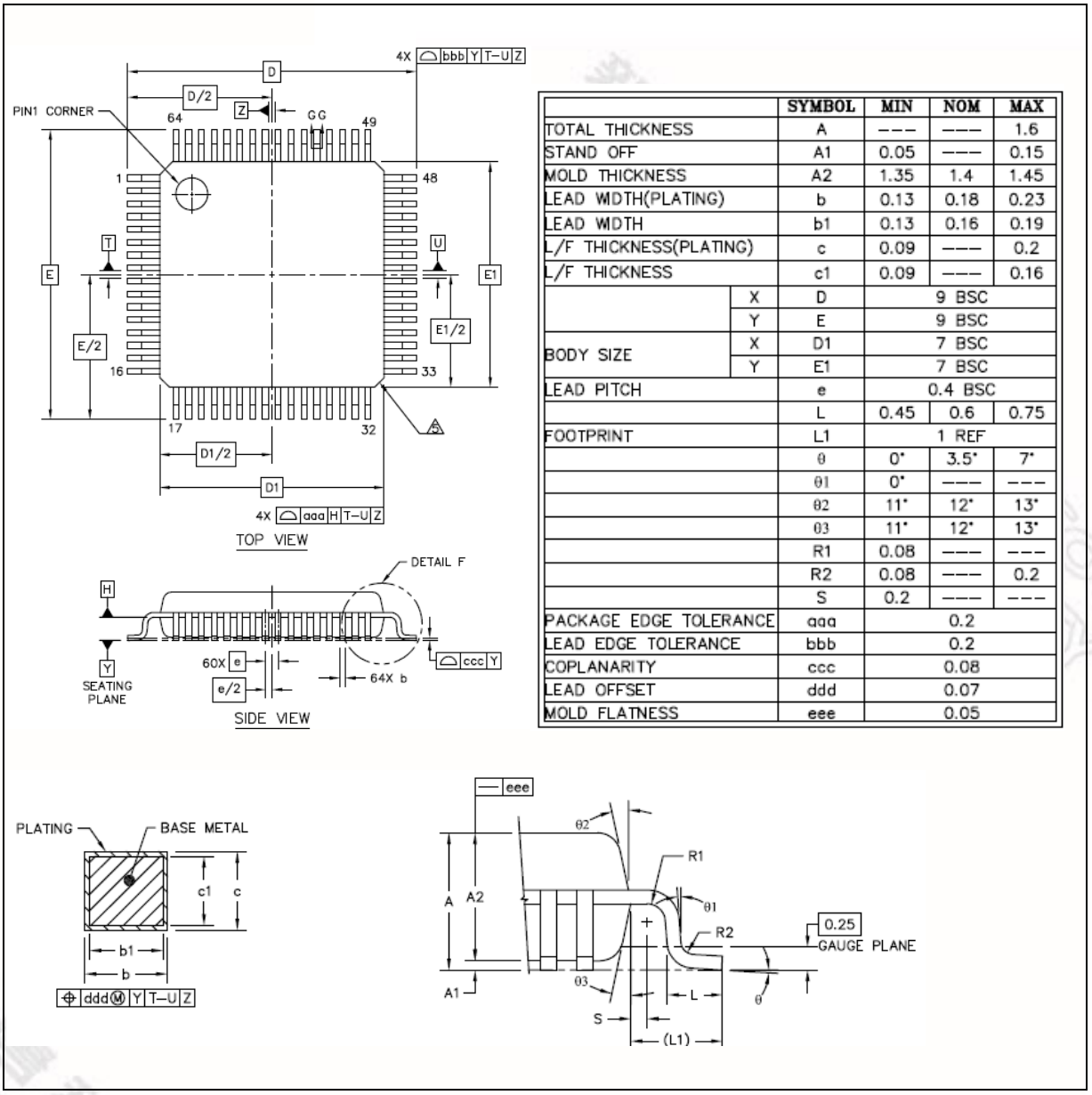
5.1 100-pin LQFP (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

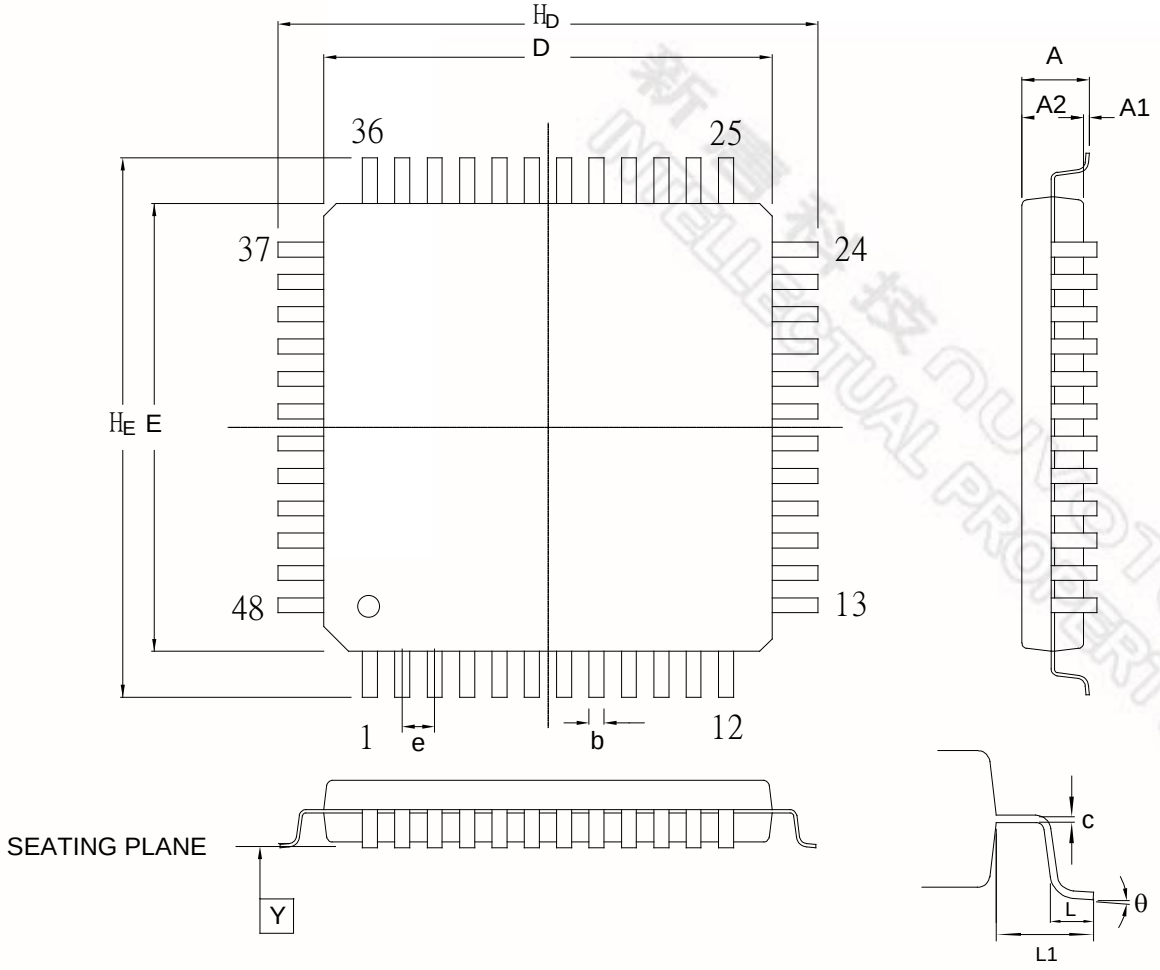
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

5.2 64-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

5.3 48-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

6 REVISION HISTORY

Revision	Date	Description
1.00	Apr. 22, 2014	First version

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

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