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APPLICATION NOTE 4096

Rise-Time Accelerator Circuit for 2-Wire Bus Applications

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Abstract: Applications that include a 2-wire bus—such as I²C or SMBus™—necessitate tradeoffs between rise time, power consumption, and noise immunity. Because the rise time for low-to-high transitions on such open-drain buses is determined by pullup resistors and bus capacitance, it is difficult to maintain clean, fast edges as you add peripherals, routing traces, and connectors. To address these rise-time problems, this application note presents a rise-time accelerator circuit that offers a simple way to speed rise time, improve noise immunity, and minimize power dissipation.

Circuit Description

In some 2-wire bus applications, correctly sized pullup resistors provide a rise time fast enough for good noise immunity along with acceptable power consumption. However, larger systems with high bus capacitance, or portable systems with stringent power requirements, may require an active circuit to achieve shorter rise times for an open-drain signal.

Figure 1 illustrates a rise-time accelerator circuit that uses the MAX3373 to speed rise time while improving noise immunity and minimizing power dissipation. The MAX3373 low-voltage level translator is used here for its ability to accelerate rise time, rather than its capability as a translator. When this IC detects a voltage rise on an I/O pin, it briefly turns on an internal strong pullup (a pFET), which quickly charges the parasitic bus capacitance. The accelerator circuit is then disabled after a short time, leaving only the internal 10kΩ pullup resistors (plus any external pullups) to maintain the high logic level.

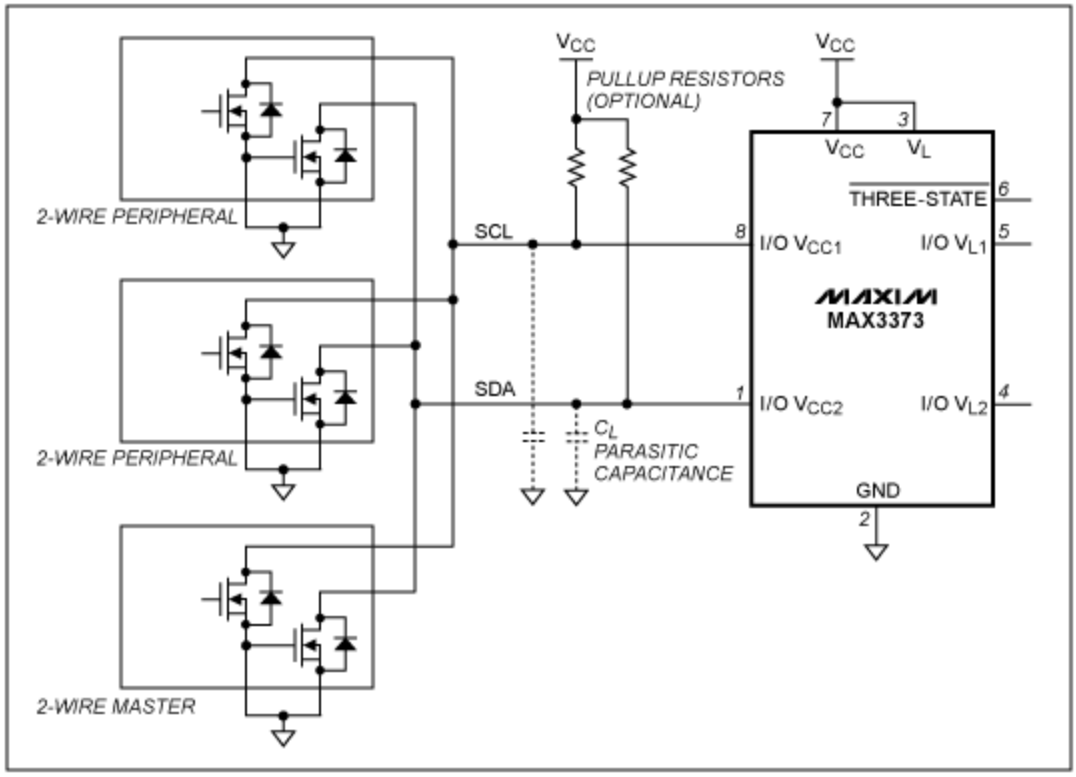

Figure 1. The MAX3373 utilizes rise-time acceleration circuitry to drive the high capacitance on a fast bus.

Performance Evaluation

The MAX3373's effectiveness as a rise-time accelerator is tested using the circuit in **Figure 2**, in which discrete open-drain FETs drive two separate lines simultaneously. Channel 1 is accelerated by the MAX3373, and Channel 2 is terminated with a simple pullup resistor and the parasitic capacitance (C is the same for both lines). The effective pullup resistance for the MAX3373 is only 5kΩ, because it includes internal 10kΩ pullup resistors on its input and output (the I/O V_{CC} and I/O V_L pins). Results are shown for the benign case of 110pF (**Figure 3**), and the maximum of 400pF allowed on an I²C bus (**Figure 4**). (Note the different time scales in these figures.)

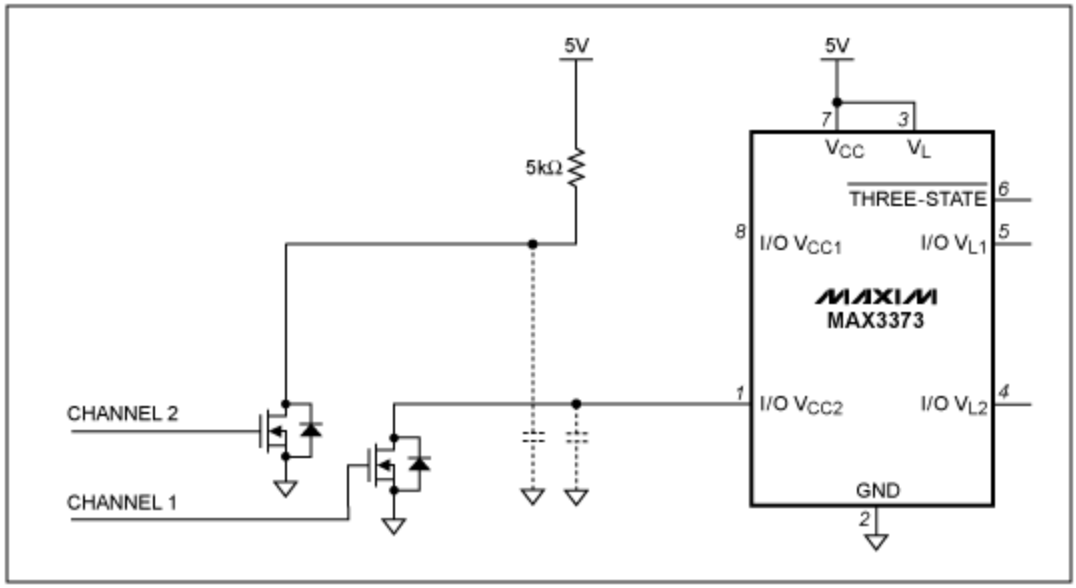

Figure 2. This circuit is used to evaluate the rise time vs. capacitance and clock rate of the MAX3373 circuit. Channel 1 utilizes the MAX3373 to accelerate the rise time, while the rise time on Channel 2 is determined by a simple pullup resistor and parasitic capacitance.

To judge the advantage gained by the MAX3373 circuit, consider the clock speeds common for 2-wire buses: 100kHz and 400kHz. At 100kHz the period is 10µs, with only 5µs in the high state. Thus, the rise time for ~110pF capacitance and a 5kΩ pullup (Figure 3) is ~1.25µs, only 12% of the period. For these conditions, the performance should be acceptable without rise-time acceleration.

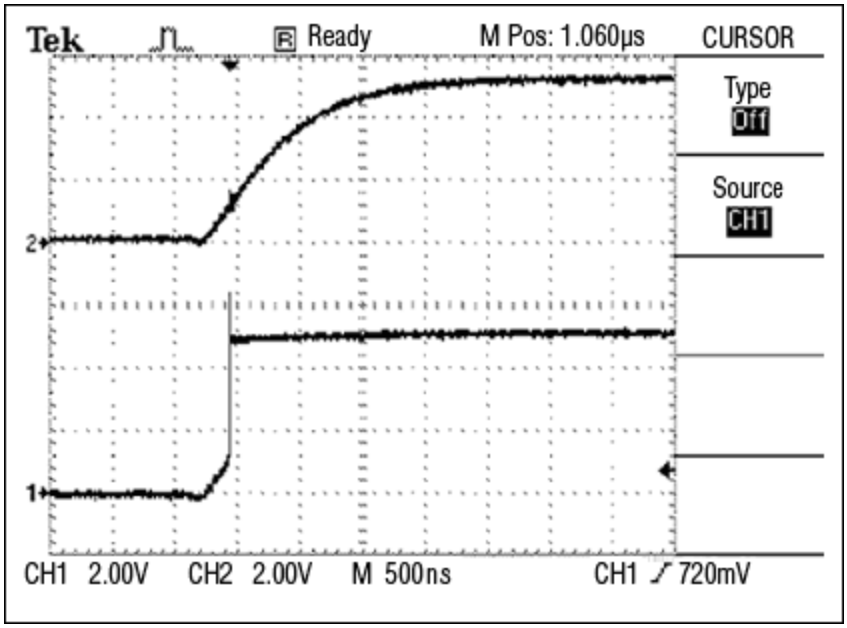

Figure 3. Illustrates the rise time of the MAX3373 circuit (Channel 1) versus the unaccelerated circuit (Channel 2), for a 5kΩ pullup, 100kHz clock, and 110pF parasitic capacitance.

For 400pF of parasitic capacitance, however, the rise time is ~4µs, which is 40% of the period and unacceptable in many 100kHz systems. Using the MAX3373 to accelerate rise time in a 400pF system

yields a 90% rise in 500ns, only 5% of the 10µs period (Figure 4).

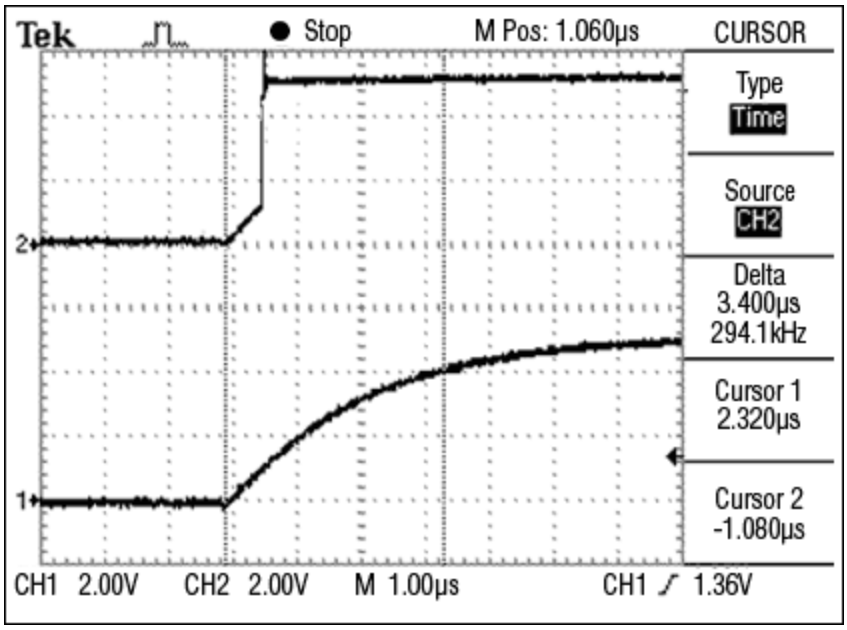

Figure 4. Illustrates the rise time of the MAX3373 circuit (Channel 1) versus the unaccelerated circuit (Channel 2), for a 5kΩ pullup, 100kHz clock, and 400pF parasitic capacitance.

For a 400kHz bus (giving a high state of 1.25µs in a 2.5µs period), the above conditions of 5kΩ and ~110pF provide a rise time of only 1.25µs, which is 50% of the period and generally unacceptable. Raising the capacitance to 400pF yields a 5µs rise time, which is double the period and clearly unacceptable. However, using the MAX3373 circuit with ~110pF load capacitance gives a 90% rise time of 250ns, only 10% of the 2.5µs period; with 400pF, it has a rise time of only ~500ns, or 20% of the period.

Summary

The use of the MAX3373 circuit as a rise-time accelerator is one of several methods for solving rise time versus clock problems on a 2-wire bus. You can speed the rise time simply by lowering the pullup resistance in some cases. The MAX3373, however, offers a simple way to speed rise times while improving noise immunity and minimizing power dissipation.

A similar article was published on *Planet Analog* (a supplement to *EE Times*) on May 24, 2006.