Keywords: BERT, T1, E1, J1, Single Chip Transceiver (SCT)

APPLICATION NOTE 3968

How to Use the Bit-Error-Rate Tester (BERT) on the DS2652x STCs

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Abstract: This application note explains how to configure the bit-error-rate tester (BERT) in the DS2652x single-chip transceivers (STCs). It details all of the choices that the designer needs to make, and gives detailed information on the registers used for each operation.

Overview

This application note describes how to use the per-channel programmable on-chip bit-error-rate tester (BERT) in the DS2652x series of T1/E1/J1 Single-Chip Transceivers (SCTs). The DS2652x devices have an internal BERT for each transceiver. This BERT can generate and detect a pseudorandom pattern, repetitive pattern, alternating (16-bit) words pattern, and Daly (modified 55 octet) pattern.

The application note also explains how to configure the DS2652x BERT to perform a bit-error-rate test. It presents all the choices to be made and gives detailed information on the registers used for each operation. The following tables show the registers involved in the BERT's configuration, control, and status.

Register	Addresses	Function
GBISR	0FA	Global BERT Interrupt Register
GBIMR	0FD	Global BERT Interrupt Mask Register
RXPC	8A	Enable for the Receiver BERT
RBPBS	8B	Bit Suppression for the Receive BERT
RBPCS1-4	D4-D7	Channels to be enabled so the Framer can accept data from the BERT pattern generator
TXPC	18A	Enable for the Transmitter BERT
TBPBS	18B	Bit Suppression for the Transmit BERT
TBPCS1-4	1D4-1D7	Channels to be enabled so the Framer can accept data from the Transmit BERT pattern generator
BAWC	1100	BERT Alternating Pattern Count Register
BRP1-4	1101-4	BERT Repetitive Pattern Set Register 1-4
BC1-2	1105-6	BERT Control 1-2
BBC1-4	1107-A	BERT Bit Counter 1-4

BEC1-3	110B-D	BERT Error Counter 1-3
BLSR	110E	BERT Status Registers
BSIM	110F	BERT Interrupt Mask

The configuration for the BERT in the DS2652x devices follows:

1. BERT setup: Configure TXPC (0x18A) and RXPC (0x08A) to enable the BERT and set up the BERT direction. If the device is in T1 mode, configure the BERT for framed or unframed operation as well.
2. Channel assignment: The BERT can be assigned on a per-channel basis for both transmitter and receiver. Any of the CH1 through CH 24 bits in TBPCS1-4 (0x1D4-1D7) and RBPCS1-4 (0x0D4-0D7) will enable the TBP_CLK/RBP_CLK for the associated channel time.
3. BERT pattern: Configure BC1.PS[2-0] (0x1105) for the desired BERT pattern with the other registers settings. (See details in tables below.) For a single bit-error test, the BC2.SBE and BC2.E1B0-2 (0x1106) can be used.

BERT Pattern Select

PS2	PS1	PS0	Pattern Definition
0	0	0	Pseudorandom 2E7–1
0	0	1	Pseudorandom 2E11–1
0	1	0	Pseudorandom 2E15–1
0	1	1	Pseudorandom Pattern QRSS. A 2^{20}: one pattern with 14 consecutive zero restriction
1	0	0	Repetitive Pattern
1	0	1	Alternating Word Pattern
1	1	0	Modified 55 Octet (Daly) Pattern. The Daly pattern is a repeating 55 octet pattern that is byte-aligned into the active DS0 time slots. The pattern is defined in an ATIS (Alliance for Telecommunications Industry Solutions) Committee T1 Technical Report Number 25 (November 1993).
1	1	1	Pseudo-Random 2E-9-1

BERT Pattern Setting

Patterns	Configuration
Pseudorandom	The BRP1-BRP4 (0x1101-0x1104) registers should all be set to 0xFF.
Repetitive	Load the pattern into BRP1-BRP4 (0x1101-0x1104) and set the pattern length in BC2.RPL[3:0] (0x1106). If the pattern is less than 32 bits, the pattern should be repeated until all 32 bits are used to describe the pattern.
Repetitive word	One word should be loaded into BRP1-BRP2 (0x1101-0x1102) and the other word should be loaded into BRP3-BRP4 (0x1103-0x1104). The BAWC register (0x1100) also needs to be set to the number of times that each word repeats.

BERT Repetitive Pattern Length Select

LENGTH (BITS)	RPL3	RPL2	RPL1	RPL0
17	0	0	0	0
18	0	0	0	1
19	0	0	1	0

20	0	0	1	1
21	0	1	0	0
22	0	1	0	1
23	0	1	1	0
24	0	1	1	1
25	1	0	0	0
26	1	0	0	1
27	1	0	1	0
28	1	0	1	1
29	1	1	0	0
30	1	1	0	1
31	1	1	1	0
32	1	1	1	1

4. Load pattern: Toggle the BC1.TC (0xE0) bit from low to high to load the pattern into the BERT transmitter.
5. Force resynchronization: Toggle the BC1.RESYNC (0xE0) bit from low to high whenever the host wishes to acquire synchronization on a new pattern. This bit must be cleared and set again for a subsequent resynchronization.
6. Test option: The BERT receiver can generate interrupts for different events. Select the event with the BSIM (0x110F) register. The software must read the BLSR (0x110E) register to determine which event(s) has occurred.
7. Clear counters: Toggle the BC1.LC bit (0x1105) from low to high to clear error counters, since the DS2652x BERT only uses latched status bits which clear after being serviced. This action resets and starts a new bit and error count cycle. It also latches the current bit count into the BERT bit count registers and current error count into the BERT error count registers, which at this point contain garbage values and should be ignored.
8. Check status: Toggle the BC1.LC bit (0x1105) from low to high again. This action latches the current bit count into the BBC1-BBC4 (0x1107-0x110A) and BEC1-BEC3 (0x110B-0x110D) registers. These two registers will increment for each data bit received, except for data received out of synchronization. These two values contain the statistical information about the BERT test and also reset the counters. Notice that the BRLOS and BSYNC bits in the BLSR register only report the synchronization condition since the last time they were cleared and not the current condition. To obtain the latest synchronization condition, check the increment of the BBC register as it is the only resource for the DS2652x devices. For longer test periods, it will be necessary to store these values in external memory, because the new values would just be added to previously stored values.

The DS2652x devices have a separate detector for all ones and all zeros. This detector should be used to qualify the pseudorandom pattern that is received. All pseudorandom pattern detectors will synchronize to either an all-one or all-zero pattern depending on the type of detector. It is mathematically impossible to prevent that situation or check that an all-ones or all-zeros pattern is no longer present. In this situation, the RDS0M (0x60) and RDS0SEL (0x12) monitor registers can be used to verify the pattern against the received all zeroes.

Conclusion

If you have further questions about our DS2652x series T1/E1/J1 SCT products, please contact the

Telecommunication Applications support team by email at: telecom.support@maximintegrated.com or call (01) 972-371-6555.

Related Parts		
DS26521	Single T1/E1/J1 Transceiver	Free Samples
DS26522	Dual T1/E1/J1 Transceiver	Free Samples
DS26524	Quad T1/E1/J1 Transceiver	Free Samples
DS26528	Octal T1/E1/J1 Transceiver	Free Samples

More Information
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