

P-Channel 20-V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---------------------|------------------------------------|--------------------|-----------------------|
| V _{DS} (V) | R _{DS(on)} (Ω) | I _D (A) | Q _g (Typ.) |
| - 20 | 0.032 at V _{GS} = - 4.5 V | - 7.1 | 16.5 |
| | 0.040 at V _{GS} = - 2.5 V | - 6.4 | |
| | 0.053 at V _{GS} = - 1.8 V | - 5.5 | |

FEATURES

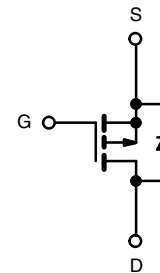
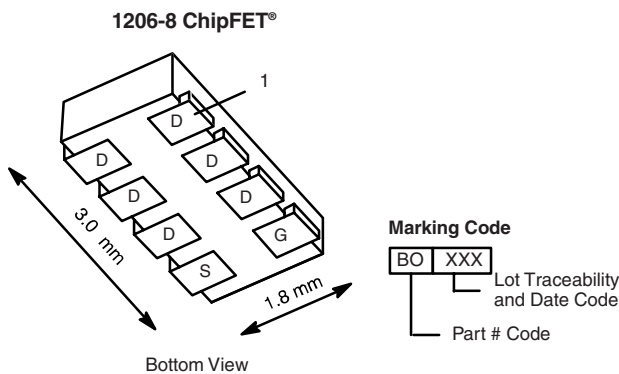
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- Ultra-Low On-Resistance
- Thermally Enhanced ChipFET® Package
- 40 % Smaller Footprint than TSOP-6



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switch, PA Switch, and Battery Switch for Portable Devices



P-Channel MOSFET

Ordering Information: Si5401DC-T1-E3 (Lead (Pb)-free)
Si5401DC-T1-GE3 (Lead (Pb)-free and Halogen-free)

| ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted | | | | |
|---|-----------------------------------|------------------------|--------------|-------|
| Parameter | Symbol | 5 s | Steady State | Unit |
| Drain-Source Voltage | V _{DS} | - 20 | | V |
| Gate-Source Voltage | V _{GS} | ± 8 | | |
| Continuous Drain Current (T _J = 150 °C) ^a | I _D | T _A = 25 °C | - 7.1 | - 5.2 |
| | | T _A = 85 °C | - 5.1 | - 3.7 |
| Pulsed Drain Current | I _{DM} | - 20 | | A |
| Continuous Source Current ^a | I _S | - 2.1 | - 1.1 | |
| Maximum Power Dissipation ^a | P _D | T _A = 25 °C | 2.5 | 1.3 |
| | | T _A = 85 °C | 1.3 | 0.7 |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to 150 | | °C |
| Soldering Recommendations (Peak Temperature) ^{b, c} | | 260 | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|--|-------------------|--------------|---------|------|------|
| Parameter | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient ^a | R _{thJA} | t ≤ 5 s | 40 | 50 | °C/W |
| | | Steady State | 80 | 95 | |
| Maximum Junction-to-Foot (Drain) | R _{thJF} | 15 | 20 | | |

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

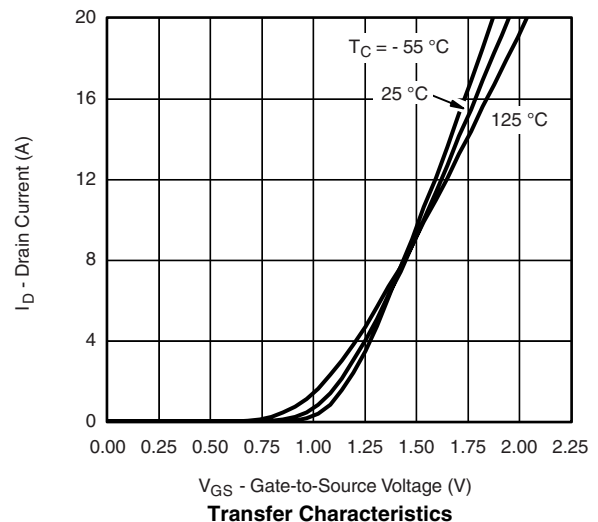
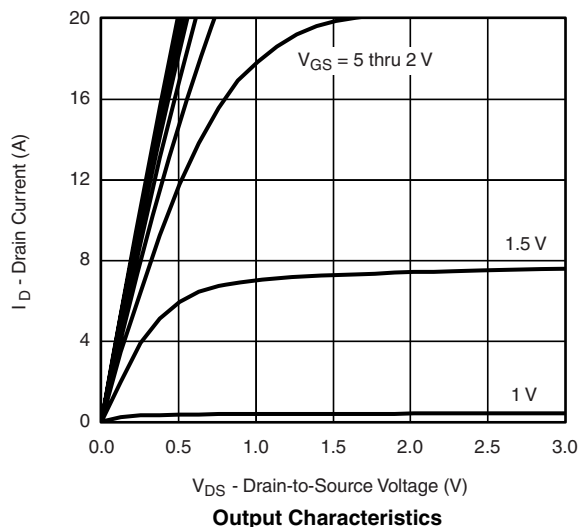
| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | |
|---|--------------|--|-------|-------|-----------|---------------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$ | -0.40 | | -1.0 | V |
| Gate-Body Leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$ | | | -1 | μA |
| | | $V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$ | | | -5 | |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$ | -20 | | | A |
| Drain-Source On-State Resistance ^a | $R_{DS(on)}$ | $V_{GS} = -4.5\text{ V}, I_D = -5.2\text{ A}$ | | 0.026 | 0.032 | Ω |
| | | $V_{GS} = -2.5\text{ V}, I_D = -4.6\text{ A}$ | | 0.033 | 0.040 | |
| | | $V_{GS} = -1.8\text{ V}, I_D = -1.9\text{ A}$ | | 0.044 | 0.053 | |
| Forward Transconductance ^a | g_{fs} | $V_{DS} = -10\text{ V}, I_D = -5.2\text{ A}$ | | 20 | | S |
| Diode Forward Voltage ^a | V_{SD} | $I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}$ | | -0.8 | -1.2 | V |
| Dynamic^b | | | | | | |
| Total Gate Charge | Q_g | $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5.2\text{ A}$ | | 16.5 | 25 | nC |
| Gate-Source Charge | Q_{gs} | | 1.7 | | | |
| Gate-Drain Charge | Q_{gd} | | 3.5 | | | |
| Gate Resistance | R_g | $f = 1\text{ MHz}$ | | 9 | | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$ | | 10 | 15 | ns |
| Rise Time | t_r | | 25 | 40 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | 115 | 175 | | |
| Fall Time | t_f | | 70 | 105 | | |
| Source-Drain Reverse Recovery Time | t_{rr} | $I_F = -1.1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$ | | 30 | 60 | nC |
| Reverse Recovery Charge | Q_{rr} | | | 140 | | |

Notes:

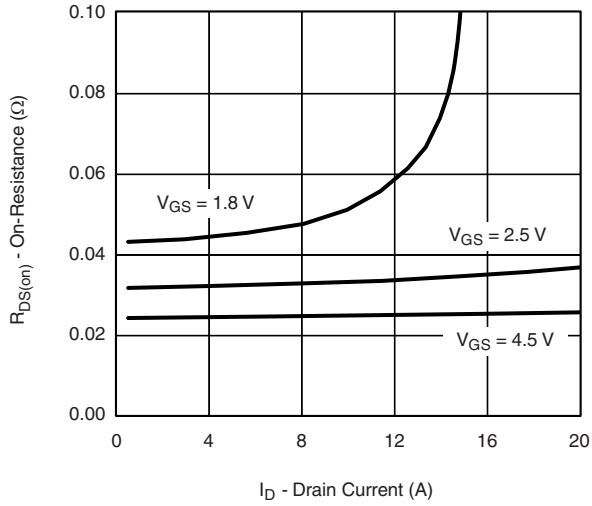
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

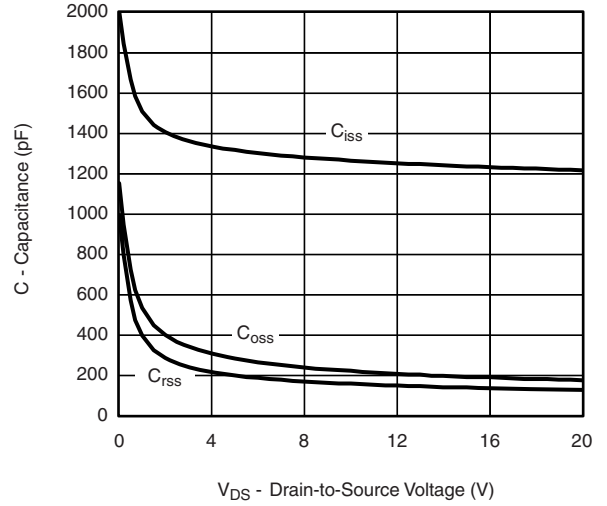
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



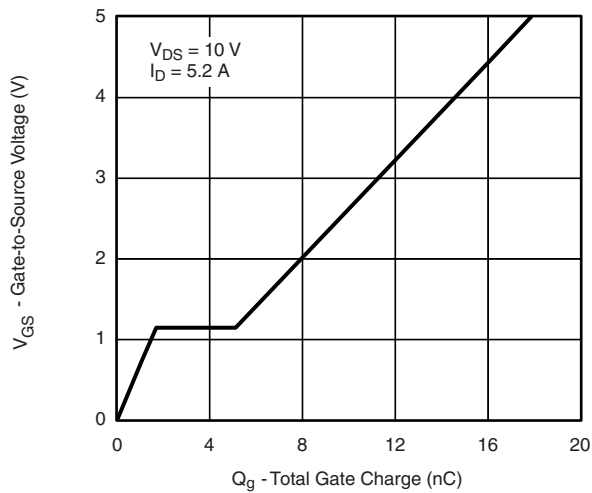
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



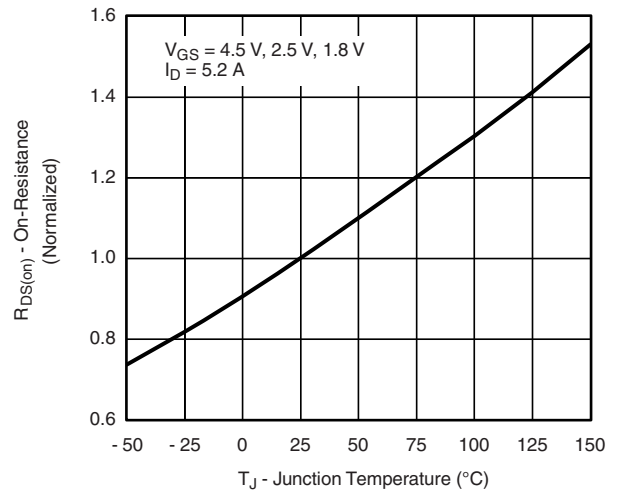
On-Resistance vs. Drain Current



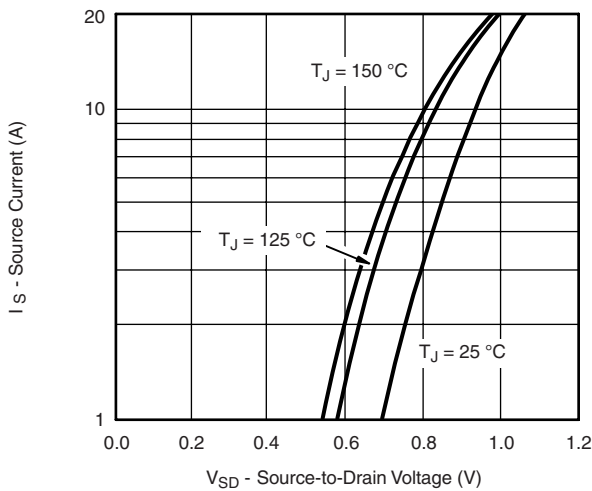
Capacitance



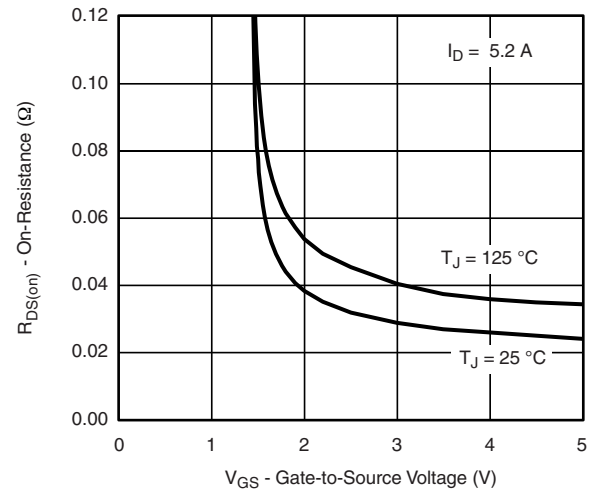
Gate Charge



On-Resistance vs. Junction Temperature

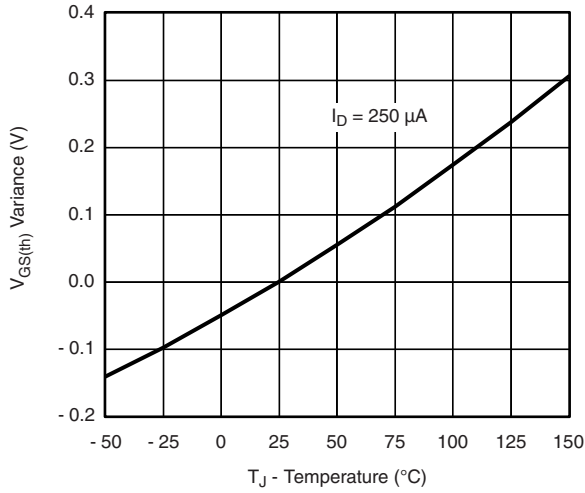


Source-Drain Diode Forward Voltage

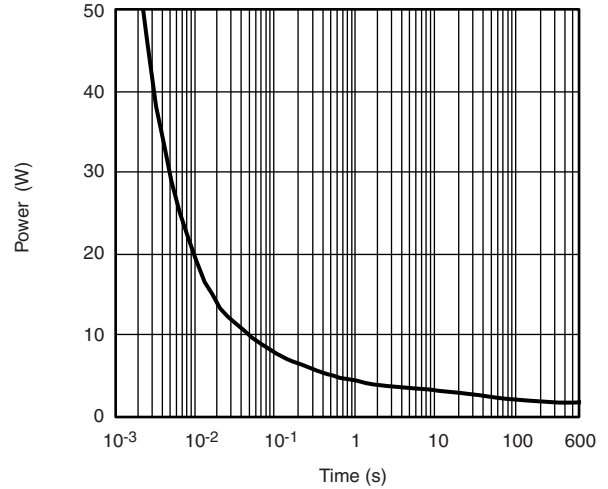


On-Resistance vs. Gate-to-Source Voltage

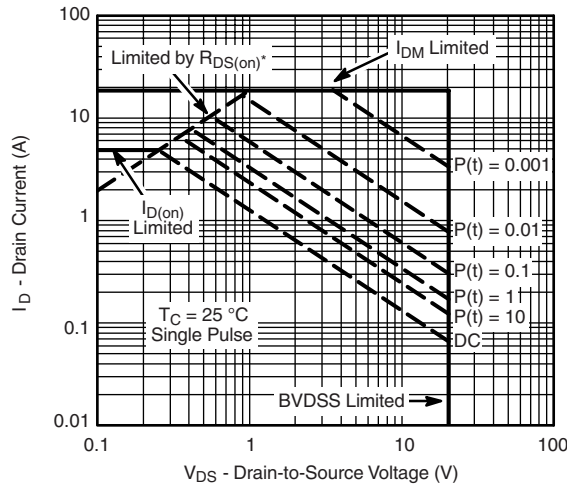
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



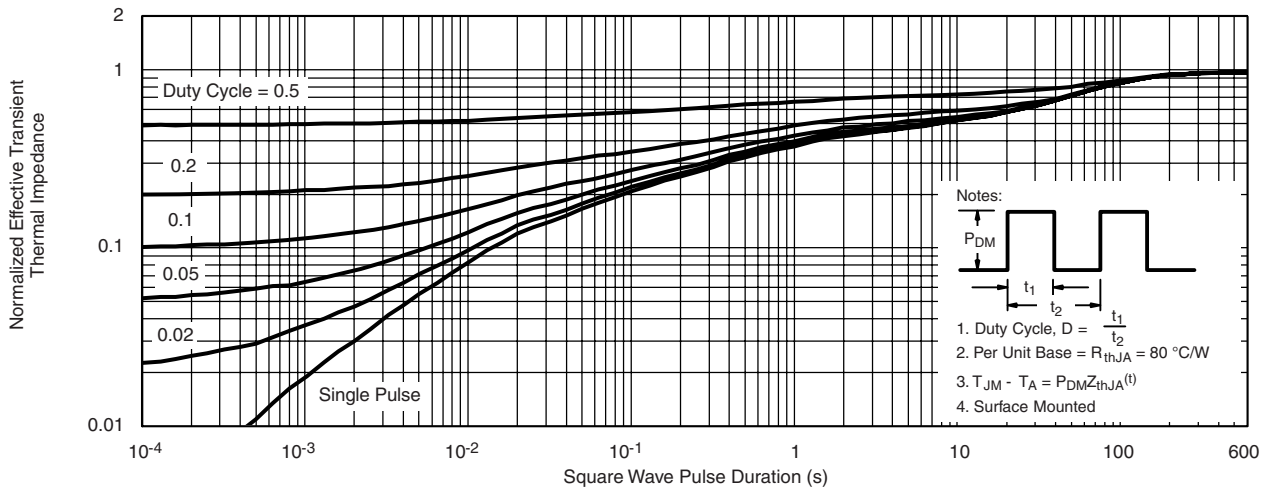
Threshold Voltage



Single Pulse Power



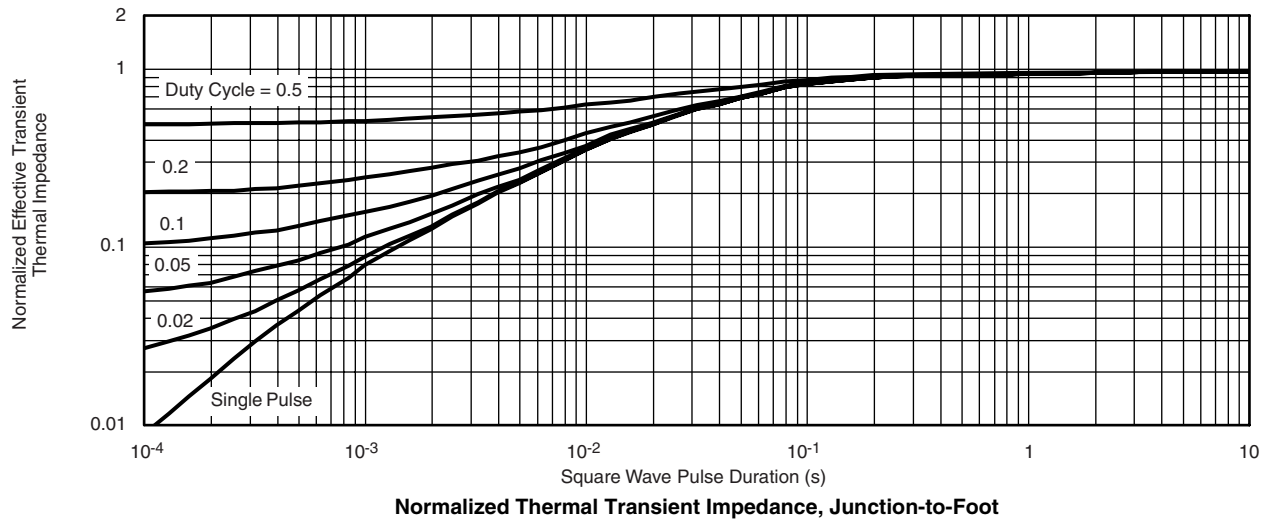
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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