14-Bit, 500 kSPS, PulSAR ADC in MSOP and LFCSP

Data Sheet **AD7946**

FEATURES

- 14-bit resolution with no missing codes
- Throughput: 500 kSPS
- INL: ±0.4 LSB typical, ±1 LSB maximum (±0.0061% of FSR)
- SINAD: 85 dB at 20 kHz
- THD: −100 dB at 20 kHz
- Pseudo differential analog input range
  - 0 V to REF with REF up to VDD
- No pipeline delay
- Single-supply 5 V operation with 1.8 V/2.5 V/3 V/5 V logic interface
- Proprietary serial interface
  - SPI-/QSPI™-/MICROWIRE™-/DSP-compatible
- Daisy-chain multiple ADCs and BUSY indicator
- Power dissipation
  - 3.3 mW at 5 V/100 kSPS
  - 3.3 µW at 5 V/100 SPS
- Standby current: 1 nA
- 10-lead MSOP (MSOP-8 size) and
  - 3 mm × 3 mm LFCSP (SOT-23 size)
- Pin-for-pin compatible with the 16-bit AD7686

APPLICATIONS

- Battery-powered equipment
- Data acquisition
- Instrumentation
- Medical instruments
- Process control

TYPICAL APPLICATION CIRCUIT

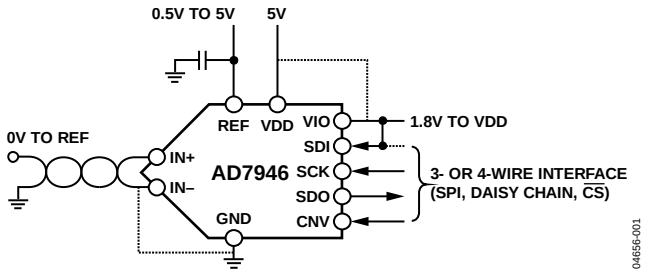

Figure 1.

GENERAL DESCRIPTION

The AD7946[1] is a 14-bit, charge redistribution, successive approximation, analog-to-digital converter (ADC) that operates from a single 5 V power supply, VDD. It contains a low power, high speed, 14-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. The part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, it samples an analog input IN+ between 0 V to REF with respect to a ground sense IN−. The reference voltage, REF, is applied externally and can be set up to the supply voltage.

Its power scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single, 3-wire bus, or it provides an optional BUSY indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate supply VIO.

The AD7946 is housed in a 10-lead MSOP or a 10-lead LFCSP with operation specified from −40°C to +85°C.

[1] Protected by U.S. Patent 6,703,961.

Table 1. MSOP, LFCSP 14-/16-/18-Bit PulSAR® ADC

Type	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	≥1000 kSPS	ADC Driver
14-Bit	AD7940	AD7942[1]	AD7946[1]		
16-Bit	AD7680	AD7685[1]	AD7686[1]	AD7980[1]	ADA4941
	AD7683	AD7687[1]	AD7688[1]	AD7983[1]	ADA4841
	AD7684	AD7694	AD7693[1]		
18-Bit		AD7691[1]	AD7690[1]	AD7982[1]	ADA4941
				AD7984[1]	ADA4841

[1] Pin-for-pin compatible.

Rev. B
Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

7/14—Rev. A to Rev. B

Replaced QFN with LFCSP ... Throughout
Changed Application Diagram Section to Typical Application Circuit Section ... 1
Changes to Product Title and Features Section ... 1
Added Note 1, General Description Section ... 1
Added EPAD Notation to Figure 5 and Table 6 ... 7
Changes to Figure 25 ... 13
Changes to Evaluating the Performance of the AD7946 Section ... 23
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

12/07—Rev. 0 to Rev. A

QFN Package Available ... Universal
Changes to Table 1 ... 1
Changes to Table 5 ... 6
Changes to Ordering Guide ... 24

7/05—Revision 0: Initial Version

SPECIFICATIONS

VDD = 4.5 V to 5.5 V, VIO = 2.3 V to VDD, REF = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	0		REF	V
Absolute Input Voltage	IN+	−0.1		VDD + 0.1	V
	IN−	−0.1		0.1	V
Analog Input CMRR	f_{IN} = 200 kHz		65		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance		See the Analog Input section			
ACCURACY					
No Missing Codes		14			Bits
Differential Linearity Error		−0.7	±0.3	+0.7	LSB[1]
Integral Linearity Error		−1	±0.4	+1	LSB
Transition Noise	REF = VDD = 5 V		0.33		LSB
Gain Error[2], T_{MIN} to T_{MAX}			±0.3	±6	LSB
Gain Error Temperature Drift			±1		ppm/°C
Offset Error[2], T_{MIN} to T_{MAX}			±0.3	±6	LSB
Offset Temperature Drift			±1		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.1		LSB
THROUGHPUT					
Conversion Rate		0		500	kSPS
Transient Response	Full-scale step			400	ns
AC ACCURACY					
Signal-to-Noise	f_{IN} = 20 kHz, REF = 5 V	84.5	85		dB[3]
	f_{IN} = 20 kHz, REF = 2.5 V		84		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		−100		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−100		dB
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz, REF = 5 V	84.5	85		dB
	f_{IN} = 20 kHz, REF = 5 V, −60 dB input		25		dB
Intermodulation Distortion[4]			100		dB

[1] LSB means least significant bit. With the 5 V input range, one LSB is 305.2 µV.
[2] See the Terminology section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.
[3] All specifications in dB are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4] f_{IN1} = 21.4 kHz, f_{IN2} = 18.9 kHz, each tone at −7 dB below full scale.

VDD = 4.5 V to 5.5 V, VIO = 2.3 V to VDD, REF = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		0.5		VDD + 0.3	V
Load Current	500 kSPS, REF = 5 V		100		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			9		MHz
Aperture Delay	VDD = 5 V		2.5		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 14-bits straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	4.5		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[1, 2]	VDD and VIO = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 5 V, 100 SPS throughput		3.3		µW
	VDD = 5 V, 100 kSPS throughput		3.3	3.8	mW
	VDD = 5 V, 500 kSPS throughput			19	mW
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact sales for extended the temperature range.

TIMING SPECIFICATIONS

T_A = −40°C to +85°C, VDD = 4.5 V to 5.5 V, VIO = 2.3 V to 5.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated.

See Figure 2 and Figure 3 for load conditions.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	0.5		1.6	µs
Acquisition Time	t_{ACQ}	400			ns
Time Between Conversions	t_{CYC}	2			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	15			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		17			ns
VIO Above 3 V		18			ns
VIO Above 2.7 V		19			ns
VIO Above 2.3 V		20			ns
SCK Low Time	t_{SCKL}	7			ns
SCK High Time	t_{SCKH}	7			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				14	ns
VIO Above 3 V				15	ns
VIO Above 2.7 V				16	ns
VIO Above 2.3 V				17	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 4.5 V				15	ns
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	15			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	3			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$				
VIO Above 4.5 V				15	ns
VIO Above 2.3 V				26	ns

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+[1], IN–[1]	GND – 0.3 V to VDD + 0.3 V or ±130 mA
REF	GND – 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
10-Lead MSOP	200°C/W
10-Lead LFCSP	48.7°C/W
θ_{JC} Thermal Impedance	
10-Lead MSOP	44°C/W
10-Lead LFCSP	2.96°C/W
Lead Temperature	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] See the Analog Input section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

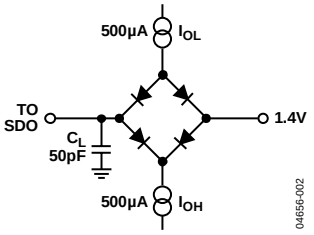


Figure 2. Load Circuit for Digital Interface Timing

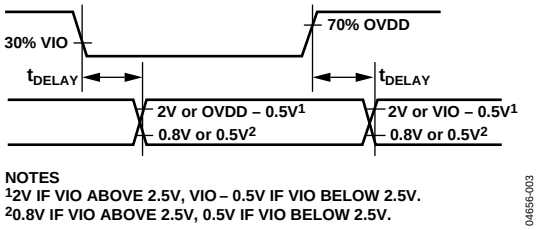


Figure 3. Voltage Levels for Timing

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

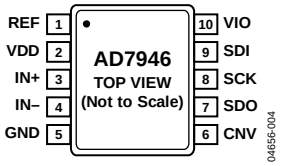


Figure 4. 10-Lead MSOP Pin Configuration

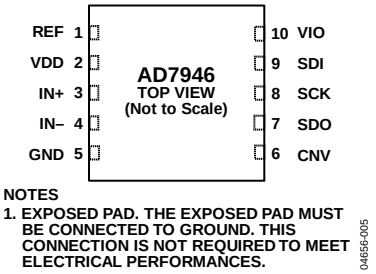


Figure 5. 10-Lead LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The REF range is from 0.5 V to VDD, and is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Analog Input. It is referred to IN–. The voltage range, that is, the difference between IN+ and IN–, is 0 V to REF.
4	IN–	AI	Analog Input Ground Sense. Connect to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode, chain, or $\overline{CS}$. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 14 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low, and if SDI or CNV is low when the conversion is complete, the BUSY indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
	EPAD	N/A	Exposed Pad. The exposed pad must be connected to ground. This connection is not required to meet electrical performances.

[1] AI = analog input, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

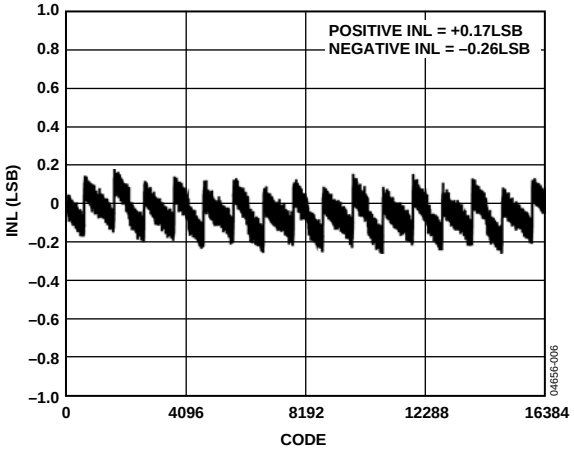


Figure 6. Integral Nonlinearity vs. Code

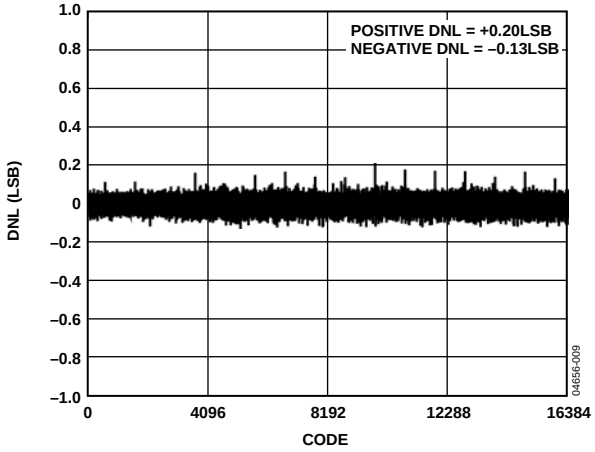


Figure 9. Differential Nonlinearity vs. Code

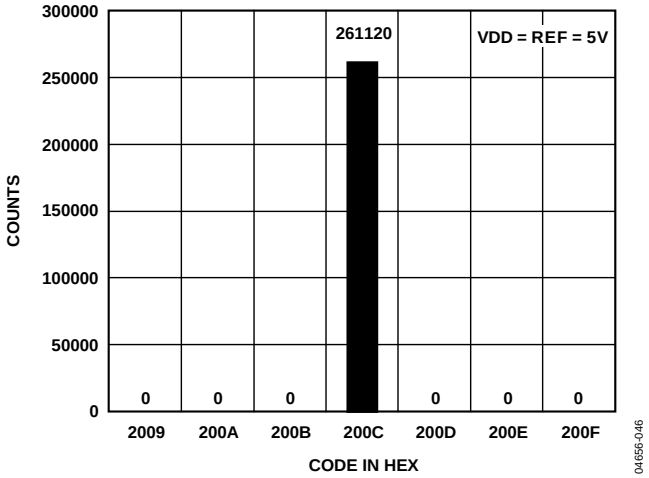


Figure 7. Histogram of a DC Input at the Code Center

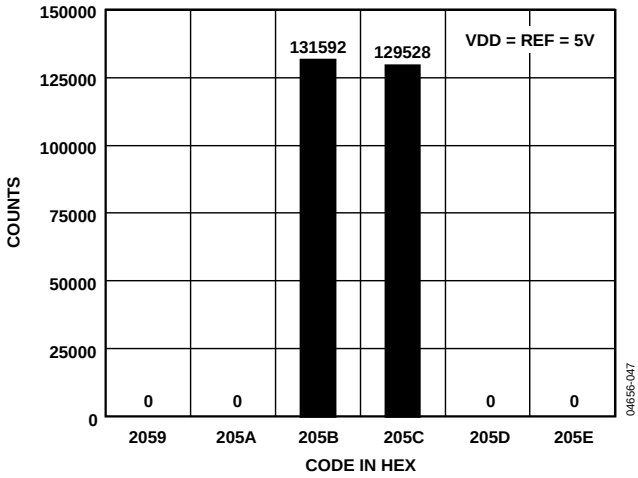


Figure 10. Histogram of a DC Input at the Code Transition

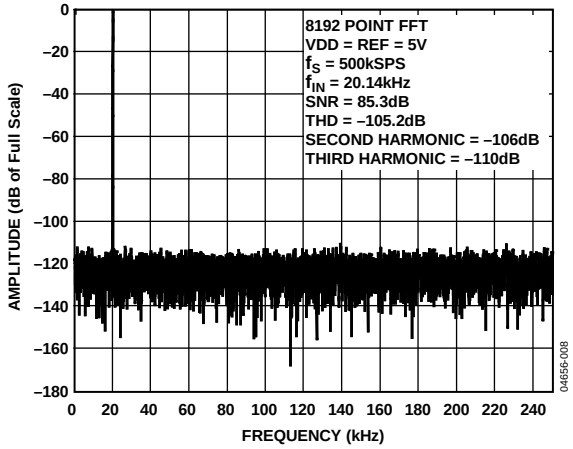


Figure 8. FFT Plot

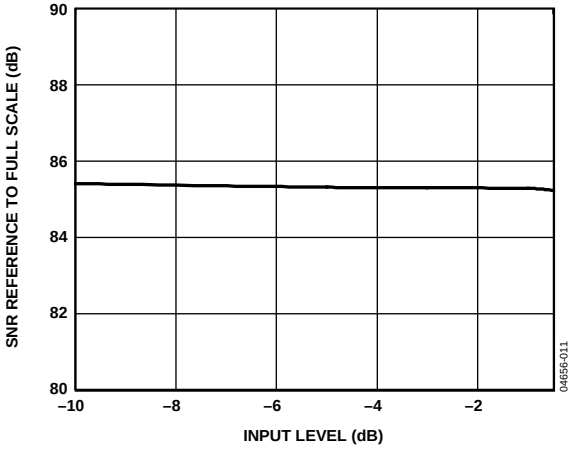


Figure 11. SNR vs. Input Level

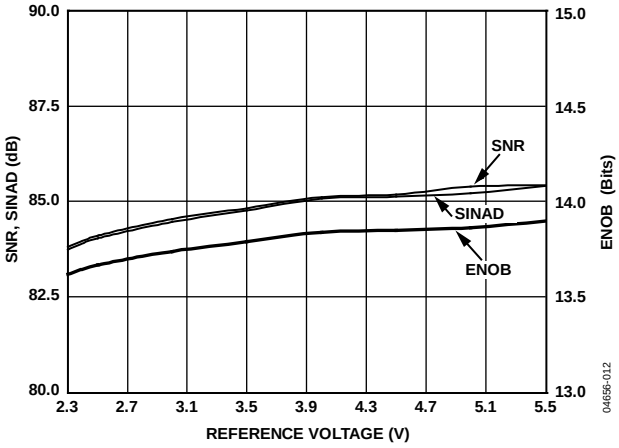


Figure 12. SNR, SINAD, and ENOB vs. Reference Voltage

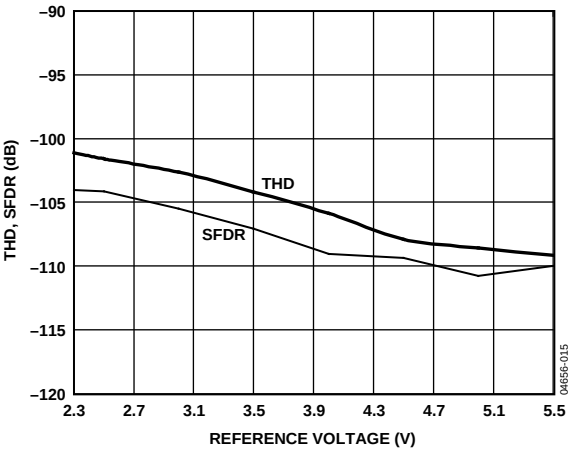


Figure 15. THD, SFDR vs. Reference Voltage

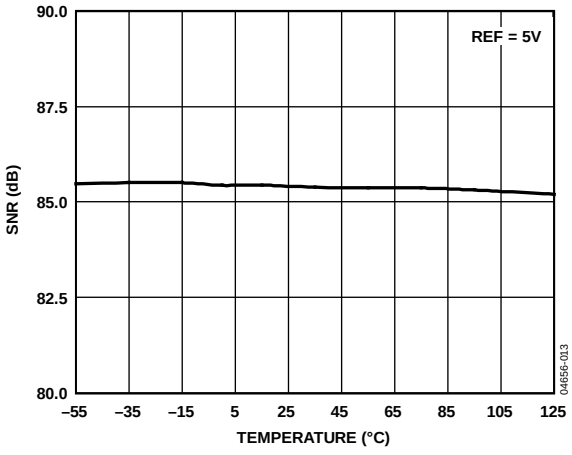


Figure 13. SNR vs. Temperature

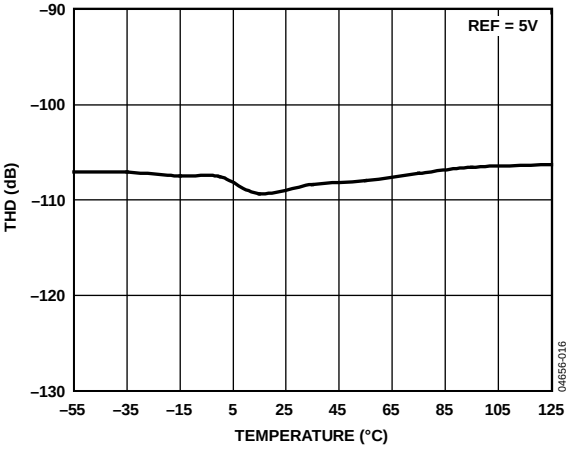


Figure 16. THD vs. Temperature

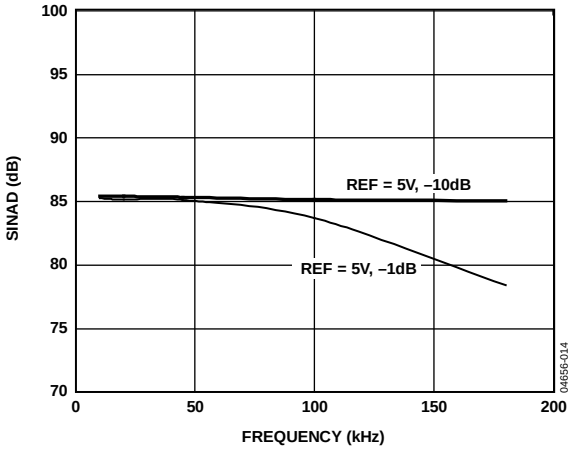


Figure 14. SINAD vs. Frequency

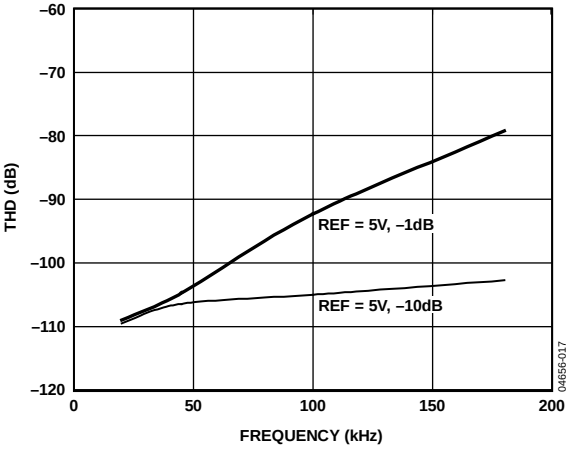


Figure 17. THD vs. Frequency

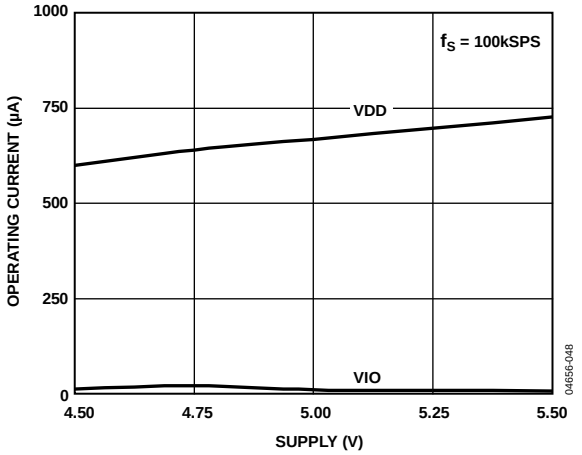


Figure 18. Operating Current vs. Supply

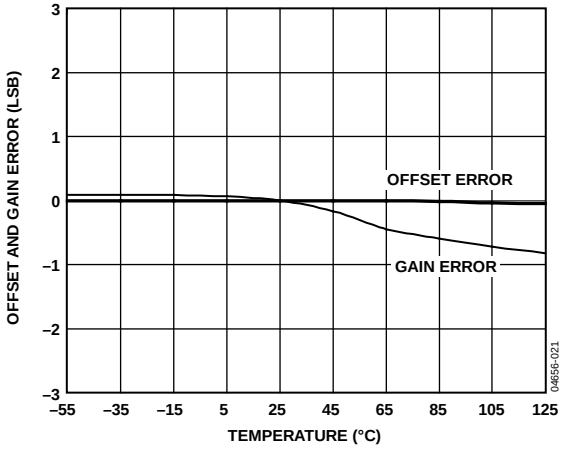


Figure 21. Offset and Gain Error vs. Temperature

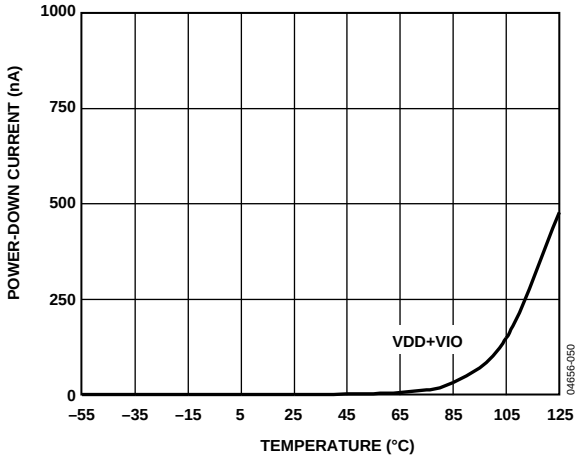


Figure 19. Power-Down Current vs. Temperature

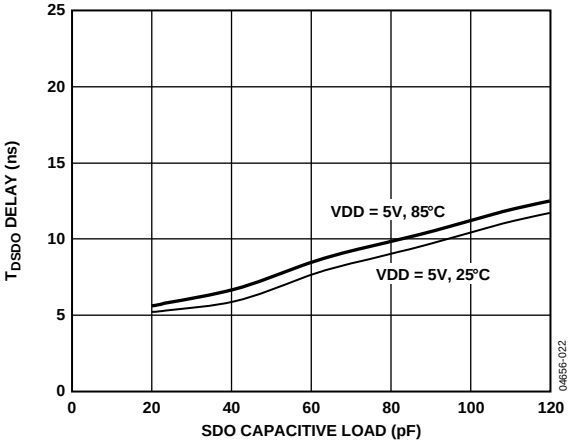


Figure 22. t_{DSDO} Delay vs. Capacitance Load and Supply

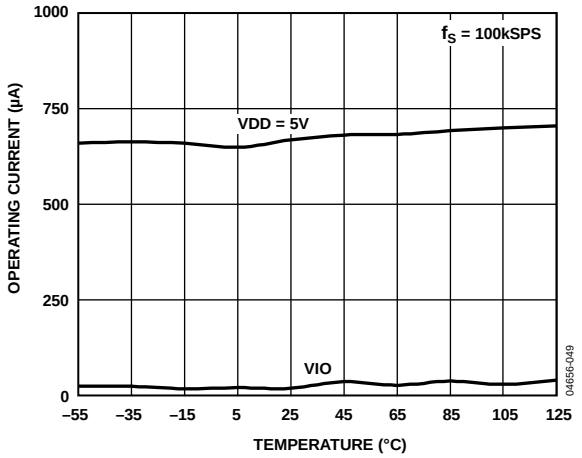


Figure 20. Operating Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (Figure 24).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level ½ LSB above analog ground (152.6 μV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111 … 10 to 111 … 11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.999542 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset has been adjusted out.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Aperture Delay
Aperture delay is the measurement of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

THEORY OF OPERATION

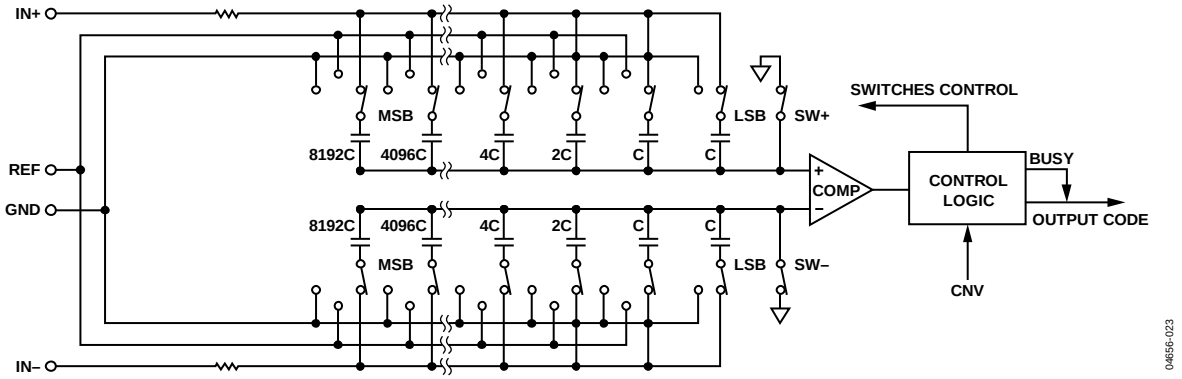


Figure 23. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7946 is a fast, low power, single-supply, precise 14-bit ADC using a successive approximation architecture.

The AD7946 can convert 500,000 samples per second (500 kSPS) and powers down between conversions. When operating at 100 SPS, for example, it consumes 3.3 µW typically, ideal for battery-powered applications.

The AD7946 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7946 is specified from 4.5 V to 5.5 V and can be interfaced to any of the 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP or a tiny 10-lead LFCSP that combines space savings and allows flexible configurations.

It is pin-for-pin compatible with the 16-bit ADC AD7686.

CONVERTER OPERATION

The AD7946 is a successive approximation ADC based on a charge redistribution DAC. Figure 23 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 14 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, the terminals of the array that are tied to the comparator's input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN− captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps (REF/2, REF/4 … REF/16,384). The control logic toggles these switches, starting with the MSB, in order to bring the comparator back into a balanced condition. After completing this process, the part returns to the acquisition phase, and the control logic generates the ADC output code and a BUSY signal indicator.

Because the AD7946 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7946 is shown in Figure 24 and Table 7.

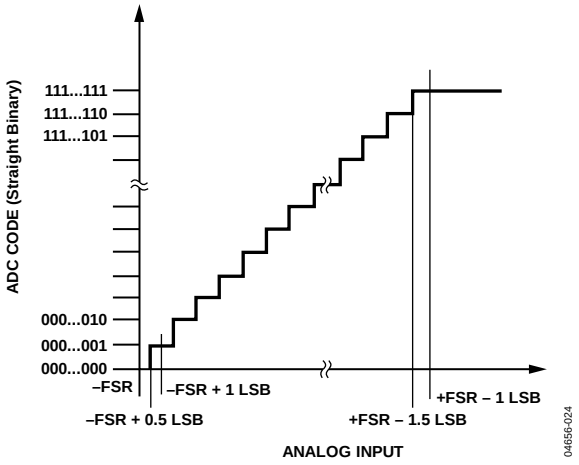


Figure 24. ADC Ideal Transfer Function

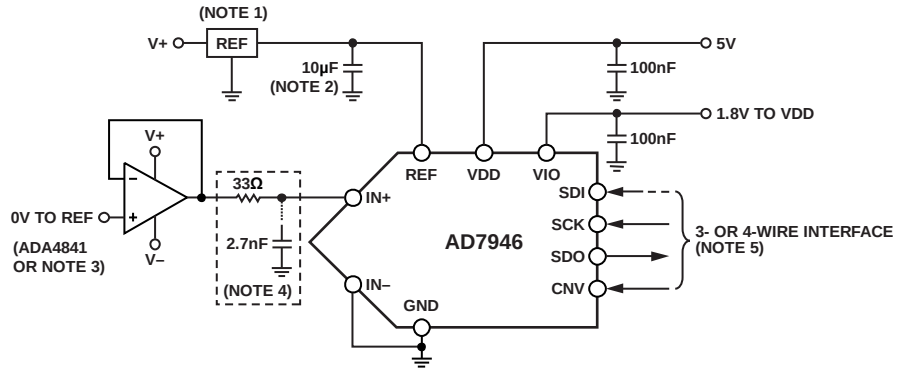
Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input REF = 5 V	Digital Output Code Hexa
FSR – 1 LSB	4.999695 V	3FFF[1]
Midscale + 1 LSB	2.500305 V	2001
Midscale	2.5 V	2000
Midscale – 1 LSB	2.499695 V	1FFF
–FSR + 1 LSB	305.2 µV	0001
–FSR	0 V	0000[2]

[1] This is also the code for an overranged analog input ($V_{IN+} - V_{IN-}$ above REF – V_{GND}).
[2] This is also the code for an underranged analog input ($V_{IN+} - V_{IN-}$ below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 25 shows an example of the recommended connection diagram for the AD7946 when multiple supplies are available.



NOTES
1. SEE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
2. C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
3. SEE DRIVER AMPLIFIER CHOICE SECTION.
4. OPTIONAL FILTER. SEE ANALOG INPUT SECTION.
5. SEE DIGITAL INTERFACE FOR MOST CONVENIENT INTERFACE MODE.

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Figure 25. Typical Application Diagram with Multiple Supplies

ANALOG INPUT

Figure 26 shows an equivalent circuit of the input structure of the AD7946.

The two diodes, D1 and D2, provide ESD protection for the analog inputs IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this causes these diodes to begin to forward-bias and start conducting current. These diodes can handle a maximum forward-biased current of 130 mA. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from VDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

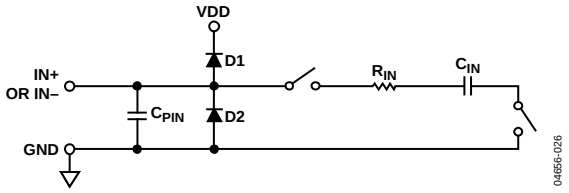

Figure 26. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the differential signal between IN+ and IN−. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 27, which represents the typical CMRR over frequency. For instance, by using IN− to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.

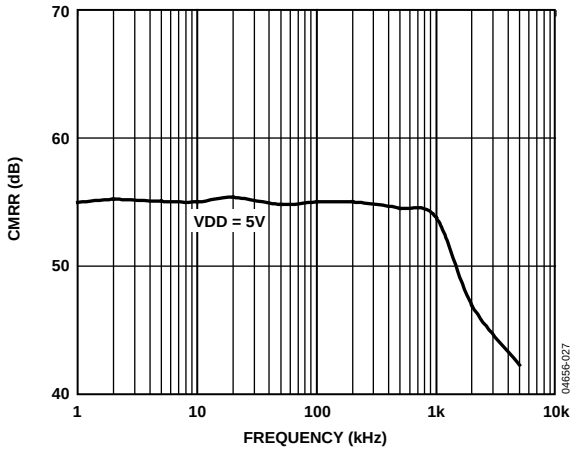

Figure 27. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 600 Ω and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter, which reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7946 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source

impedance and the maximum input frequency, as shown in Figure 28.

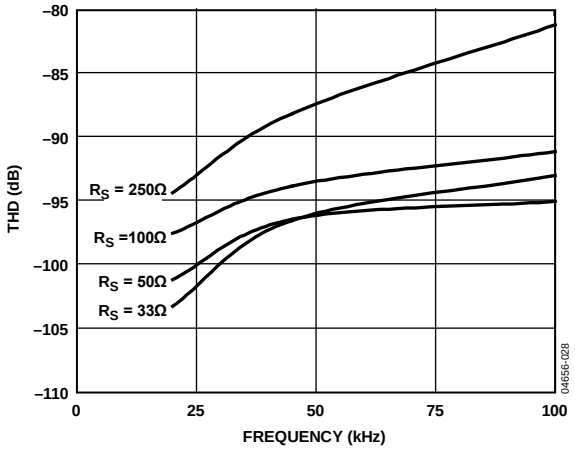

Figure 28. THD vs. Analog Input Frequency and Source Resistance

DRIVER AMPLIFIER CHOICE

Although the AD7946 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7946. Note that the AD7946 has a noise much lower than most of the other 14-bit ADCs and, therefore, can be driven by a noisier amplifier to meet a given system noise specification. The noise coming from the amplifier is filtered by the AD7946 analog input circuit 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used.
- For ac applications, the driver should have a THD performance commensurate with the AD7946. Figure 17 shows the THD vs. frequency that the driver should exceed.
- For multichannel multiplexed applications, the driver amplifier and the AD7946 analog input circuit must settle a full-scale step onto the capacitor array at a 14-bit level (0.006%). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 14-bit level and should be verified prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4841	Very low noise, small and low power
AD8021	Very low noise and high frequency
AD8655	5 V single-supply, low noise, and low power
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single-supply, low power
AD8519	Small, low power, and low frequency
AD8031	High frequency and low power

VOLTAGE REFERENCE INPUT

The AD7946 voltage reference input REF has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source, for example, a reference buffer using the AD8031 or the AD8603, a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR43x reference.

If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7946 is specified at 4.5 V to 5.5 V. It uses two power supply pins: a core supply VDD and a digital input/output interface supply VIO. VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD can be tied together. The AD7946 is independent of power supply sequencing between VIO and VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 29, which represents PSRR over frequency.

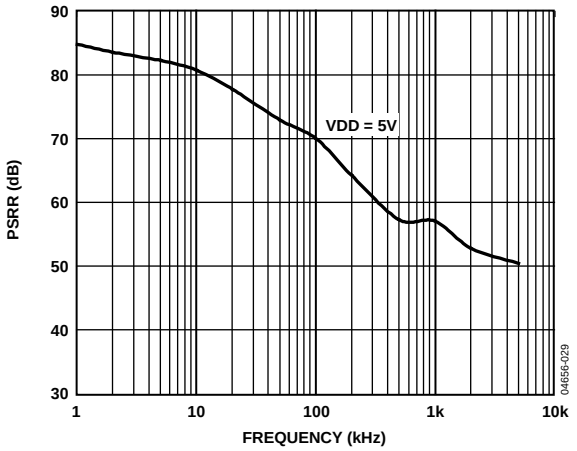

Figure 29. PSRR vs. Frequency

The AD7946 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate, as shown in Figure 30. This makes the part ideal for low sampling rate (even a few Hz) and low battery-powered applications.

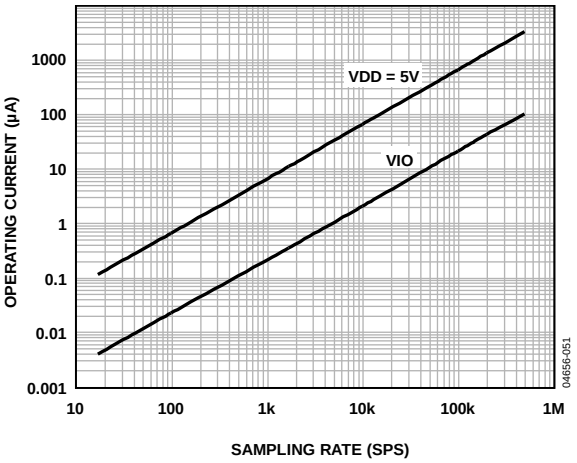

Figure 30. Operating Currents vs. Sampling Rate

SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the AD7946, with its low operating current, can be supplied directly using the reference circuit shown in Figure 31. The reference line can be driven by one of the following:

- The system power supply directly.
- A reference voltage with enough current output capability, such as the ADR43x.
- A reference buffer, such as the AD8031 or AD8603, which can also filter the system power supply, as shown in Figure 31.

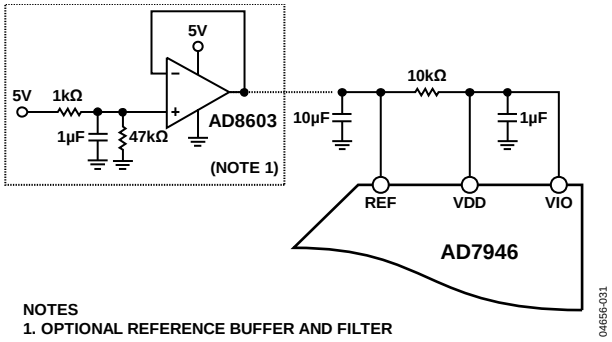

Figure 31. Example of Application Circuit

SINGLE-SUPPLY APPLICATION

Figure 32 shows a typical 14-bit single-supply application. There are different challenges to doing a single-supply, high resolution design, and the ADA4841 addresses these nicely. The combination of low noise, low power, wide input range, rail-to-rail output, and high speed make the ADA4841 a perfect driver solution for low power, single-supply 14-bit ADCs, such as the AD7946. In a single-supply system, one of the main challenges is to use the amplifier in buffer mode to have the lowest output noise and still preserve linearity compatible with the ADC. Rail-to-rail input amplifiers usually have higher noise than the ADA4841 and cannot be used on their entire input range in buffer mode because of the nonlinear region around the crossover point of their input stage. The ADA4841, which has no crossover region but has a wide linear input range from ground to 1 V below positive rail, solves this issue, as shown in Figure 32, where it can accept the 0 V to 4.096 V input range with a supply as low as 5.2 V. This supply allows using a small, low dropout, low temperature drift ADR364 reference voltage. Note that, like any rail-to-rail output amplifier at the low end of its output range close to ground, the ADA4841 can exhibit some nonlinearity on a small region of approximately 25 mV from ground. The ADA4841 drives a 1-pole, low-pass filter. This filter limits the already very low noise contribution from the amplifier to the AD7946.

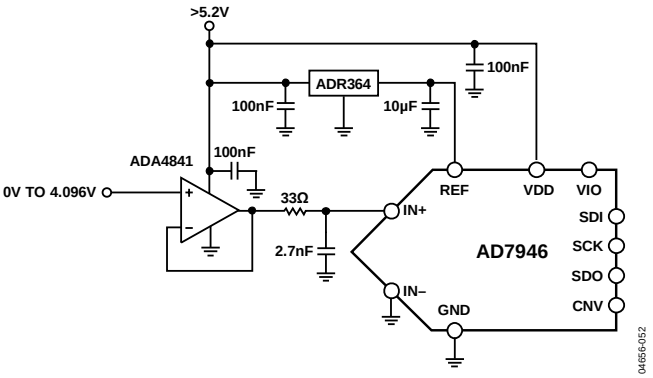

Figure 32. Example of a Single-Supply Application Circuit

DIGITAL INTERFACE

Although the AD7946 has a reduced number of pins, it offers flexibility in its serial interface modes.

The AD7946, when in $\overline{CS}$ mode, is compatible with SPI, QSPI™, digital hosts, and DSPs, for example, Blackfin® ADSP-BF53x or ADSP-219x. This interface can use either 3-wire or 4-wire. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

The AD7946, when in chain mode, provides a daisy chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The operating mode depends on the SDI level when the CNV rising edge occurs. $\overline{CS}$ mode is selected if SDI is high, and chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected, the chain mode is always selected.

In either mode, the AD7946 offers the flexibility to optionally force a start bit in front of the data bits. This start bit can be used as a BUSY signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a BUSY indicator, the user must time out the maximum conversion time prior to readback.

BUSY indicator feature is enabled

- In $\overline{CS}$ mode, if CNV or SDI is low when the ADC conversion ends (see Figure 36 and Figure 40).
- In chain mode, if SCK is high during the CNV rising edge (see Figure 44).

$\overline{CS}$ MODE 3-WIRE, NO BUSY INDICATOR

This mode is usually used when a single AD7946 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 33 and the corresponding timing is given in Figure 34.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it continues to completion irrespective of the state of CNV. For instance, it could be useful to bring CNV low to select other SPI devices, such as analog multiplexers, but CNV must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7946 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 14th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

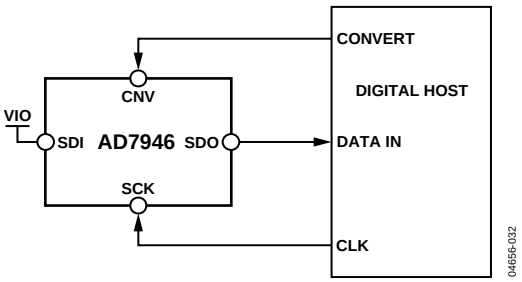

Figure 33. $\overline{CS}$ Mode 3-Wire, No BUSY Indicator Connection Diagram (SDI High)

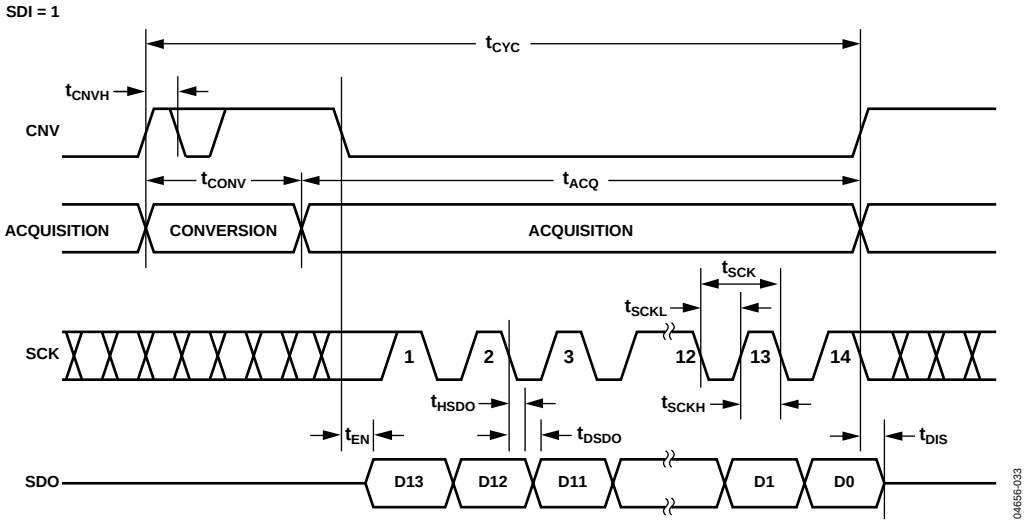

Figure 34. $\overline{CS}$ Mode 3-Wire, No BUSY Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE 3-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7946 is connected to an SPI-compatible digital host having an interrupt input.

The connection diagram is shown in Figure 35, and the corresponding timing is given in Figure 36.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV could be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7946 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 15th SCK falling edge, or when CNV goes high, whichever is earlier, SDO returns to high impedance.

If multiple AD7946s are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

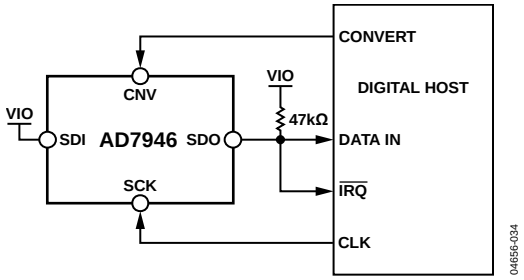

Figure 35. $\overline{CS}$ Mode 3-Wire with BUSY Indicator Connection Diagram (SDI High)

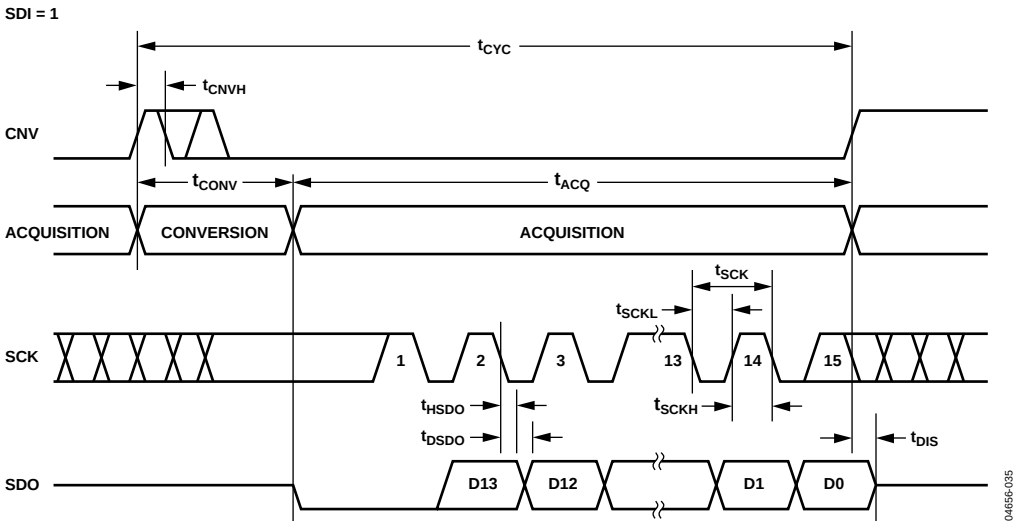

Figure 36. $\overline{CS}$ Mode 3-Wire with BUSY Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE 4-WIRE, NO BUSY INDICATOR

This mode is usually used when multiple AD7946s are connected to an SPI-compatible digital host.

A connection diagram example using two AD7946s is shown in Figure 37, and the corresponding timing is given in Figure 38.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid the generation of the BUSY signal indicator. When the conversion is complete, the AD7946 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 14th SCK falling edge, or when SDI goes high, whichever is earlier, SDO returns to high impedance and another AD7946 can be read.

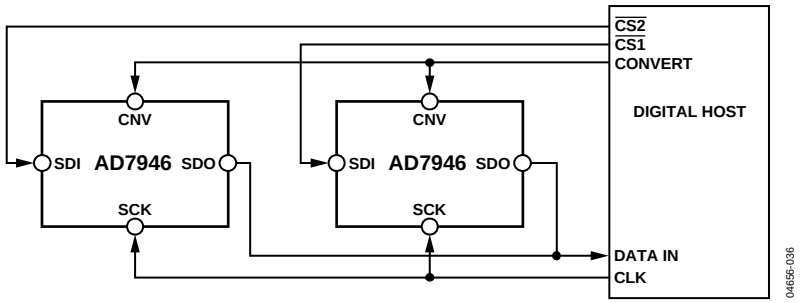

Figure 37. $\overline{CS}$ Mode 4-Wire, No BUSY Indicator Connection Diagram

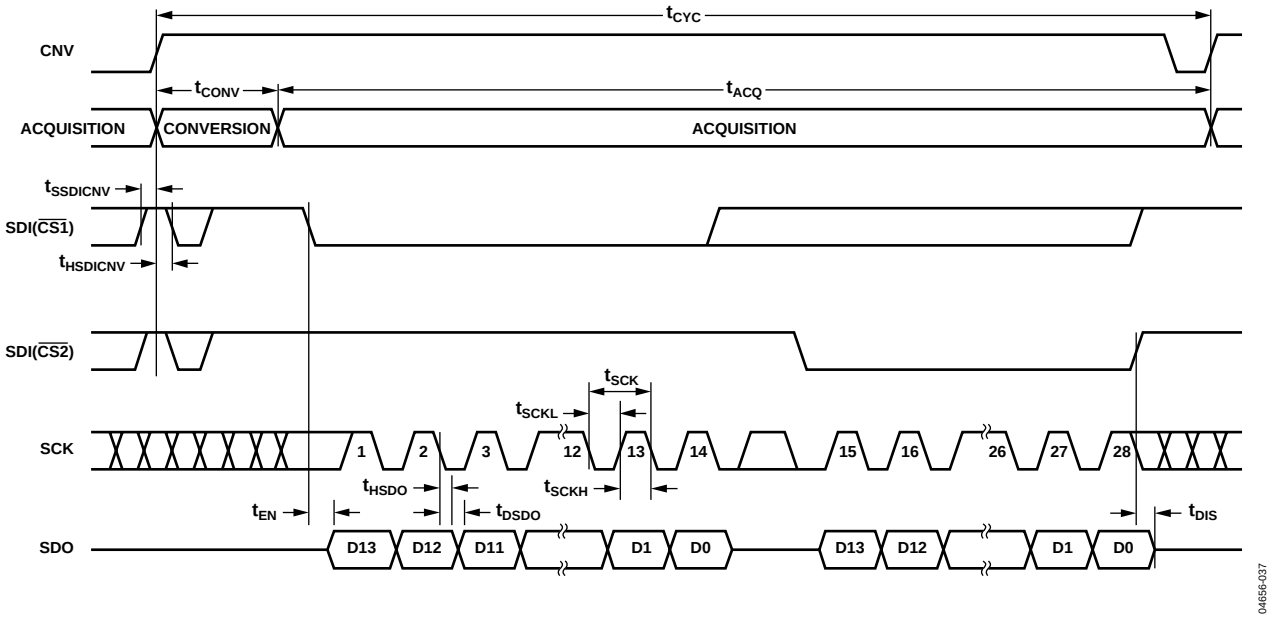

Figure 38. $\overline{CS}$ Mode 4-Wire, No BUSY Indicator Serial Interface Timing

$\overline{CS}$ MODE 4-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7946 is connected to an SPI-compatible digital host, which has an interrupt input, and it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 39, and the corresponding timing is given in Figure 40.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI could be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the BUSY signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7946 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 15th SCK falling edge or SDI going high, whichever is earlier, the SDO returns to high impedance.

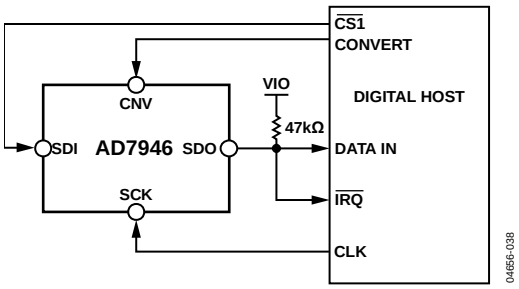

Figure 39. $\overline{CS}$ Mode 4-Wire with BUSY Indicator Connection Diagram

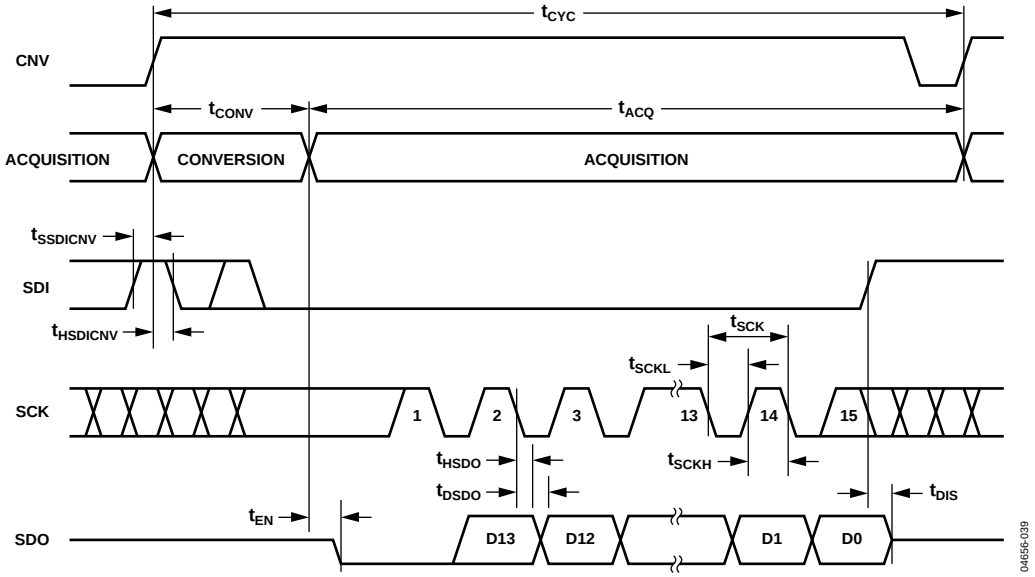

Figure 40. $\overline{CS}$ Mode 4-Wire with BUSY Indicator Serial Interface Timing

CHAIN MODE, NO BUSY INDICATOR

This mode can be used to daisy-chain multiple AD7946s on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7946s is shown in Figure 41, and the corresponding timing is given in Figure 42.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the BUSY indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO, and the AD7946 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are then clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 14 × N clocks are required to readback the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7946s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time. For instance, with a 3 ns digital host setup time and 3 V interface, up to four AD7946s running at a conversion rate of 360 kSPS can be daisy-chained on a 3-wire port.

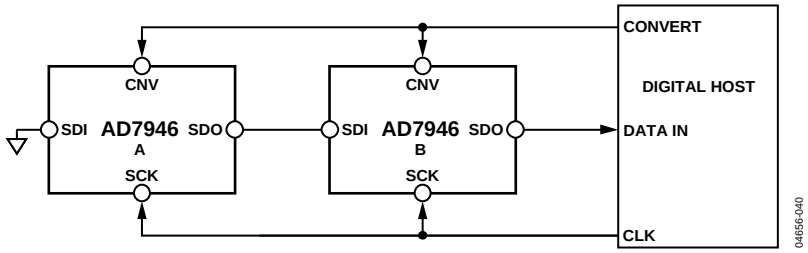

Figure 41. Chain Mode, No BUSY Indicator Connection Diagram

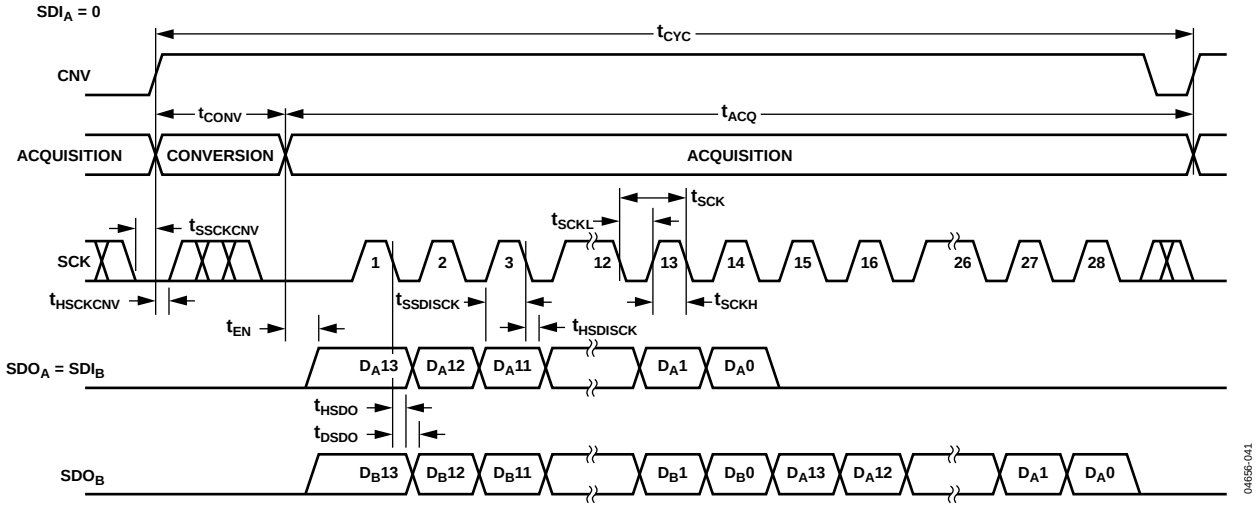

Figure 42. Chain Mode, No BUSY Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can be used to daisy-chain multiple AD7946s on a 3-wire serial interface while providing a BUSY indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using three AD7946s is shown in Figure 43, and the corresponding timing is given in Figure 44.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the BUSY indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the near-end ADC (ADC C in Figure 43) SDO is driven high. This transition on SDO can be used as a BUSY indicator to trigger the data readback controlled by the digital host. The AD7946 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are then clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 14 × N + 1 clocks are required to readback the N ADCs. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7946s in the chain, provided the digital host has an acceptable hold time. For instance, with a 3 ns digital host setup time and 3 V interface, up to four AD7946s running at a conversion rate of 360 kSPS can be daisy-chained to a single 3-wire port.

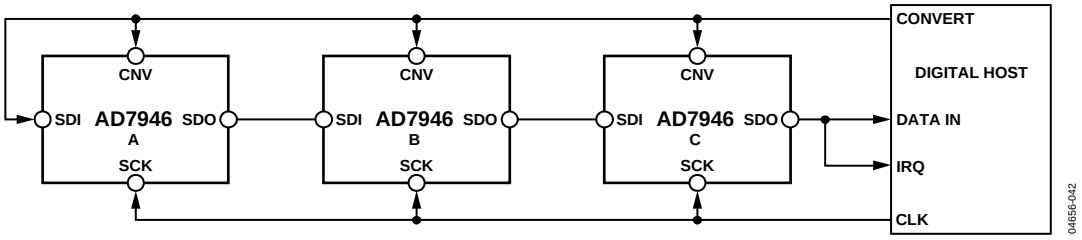

Figure 43. Chain Mode with BUSY Indicator Connection Diagram

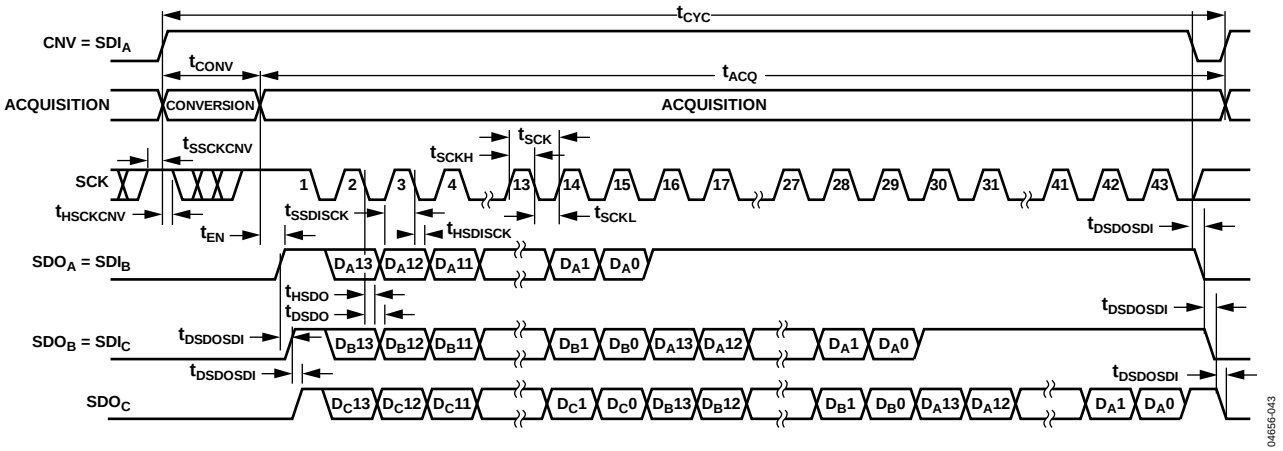

Figure 44. Chain Mode with BUSY Indicator Serial Interface Timing

APPLICATION GUIDELINES

LAYOUT

The printed circuit board that houses the AD7946 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7946, with all its analog signals on the left side and all its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7946 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It could be common or split between the digital and analog sections. In the latter case, the planes should be joined underneath the AD7946s.

The AD7946 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins and connecting it with wide, low impedance traces.

Finally, the power supplies VDD and VIO of the AD7946 should be decoupled with ceramic capacitors (typically 100 nF) placed close to the AD7946 and connected using short and wide traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

An example of layout following these rules is shown in Figure 45 and Figure 46.

EVALUATING THE PERFORMANCE OF THE AD7946

Other recommended layouts for the AD7946 are outlined in the documentation of the EVAL-AD7946SDZ evaluation board. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

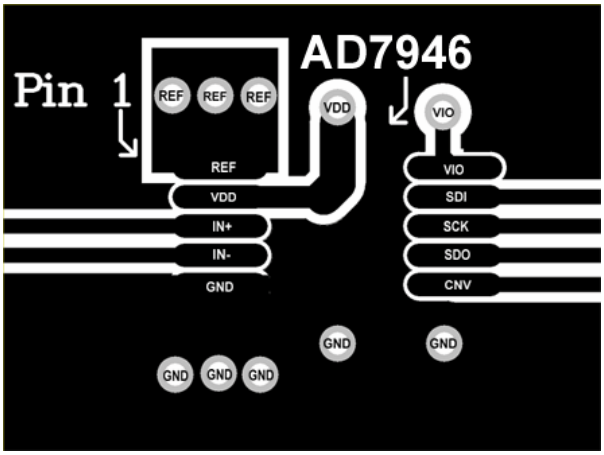

Figure 45. Example of Layout of the AD7946 (Top Layer)

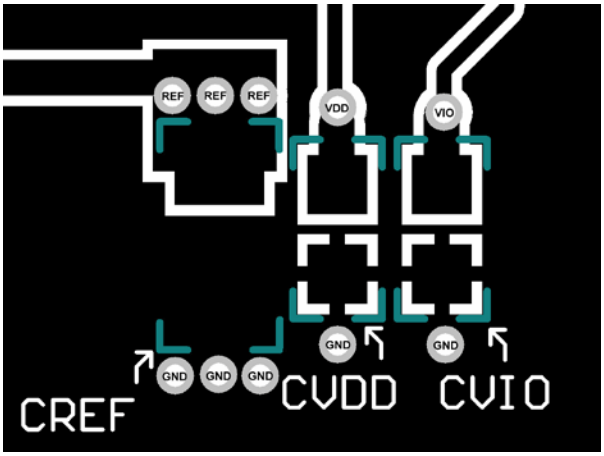

Figure 46. Example of Layout of the AD7946 (Bottom Layer)

OUTLINE DIMENSIONS

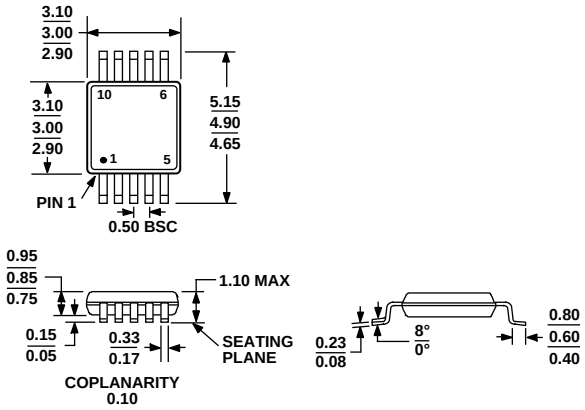

Figure 47.10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

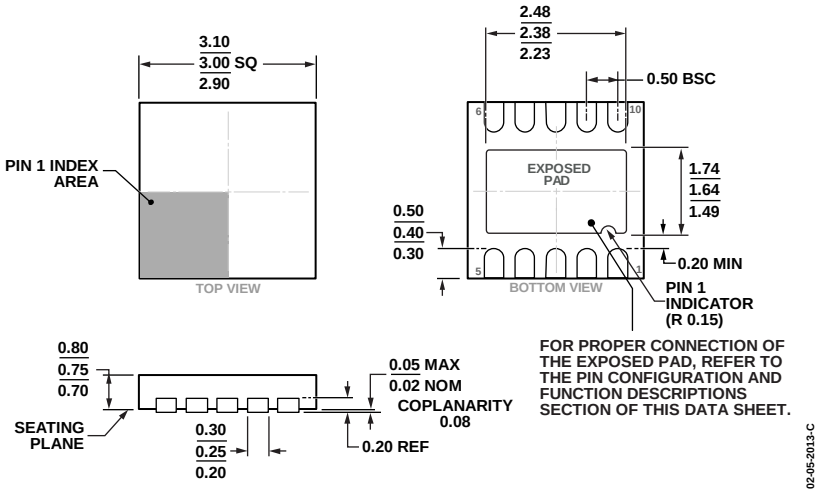

Figure 48. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead (CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
AD7946BRMZ	−40°C to +85°C	10-Lead MSOP	RM-10	Tube, 50	C4X
AD7946BRMZRL7	−40°C to +85°C	10-Lead MSOP	RM-10	Reel, 1,000	C4X
AD7946BCPZRL7	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	Reel, 1,000	C4X
AD7946BCPZRL	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	Reel, 5,000	C4X
EVAL-AD7946SDZ		Evaluation Board			
EVAL-SDP-CB1Z		Controller Board			

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7946SDZ can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation and/or demonstration purposes.
[3] The EVAL-SDP-CB1Z allows a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the SDZ designator.