

IS31AP4991

1.2W AUDIO POWER AMPLIFIER WITH ACTIVE-LOW STANDBY MODE

September 2021

GENERAL DESCRIPTION

The IS31AP4991 has been designed for demanding audio applications such as mobile phones and permits the reduction of the number of external components.

It is capable of delivering 1.2W of continuous RMS output power into an 8Ω load @ 5V.

An externally-controlled standby mode reduces the supply current to much less than 1μA. It also includes internal thermal shutdown protection.

The unity-gain stable amplifier can be configured by external gain setting resistors.

FEATURES

- Operating from $V_{CC} = 2.7V \sim 5.5V$
- 1.2W output power @ $V_{CC} = 5V$, THD+N= 1%, $f = 1kHz$, with 8Ω load
- Ultra-low consumption in standby mode (much less than 1μA)
- 65dB PSRR @217Hz in grounded mode
- Near-zero click-and-pop
- Ultra-low distortion (0.025%@0.5W, 1kHz)
- SOP-8 and MSOP-8 package

APPLICATIONS

- Mobile phones
- PDAs
- Portable electronic devices
- Notebook computer

TYPICAL APPLICATION CIRCUIT

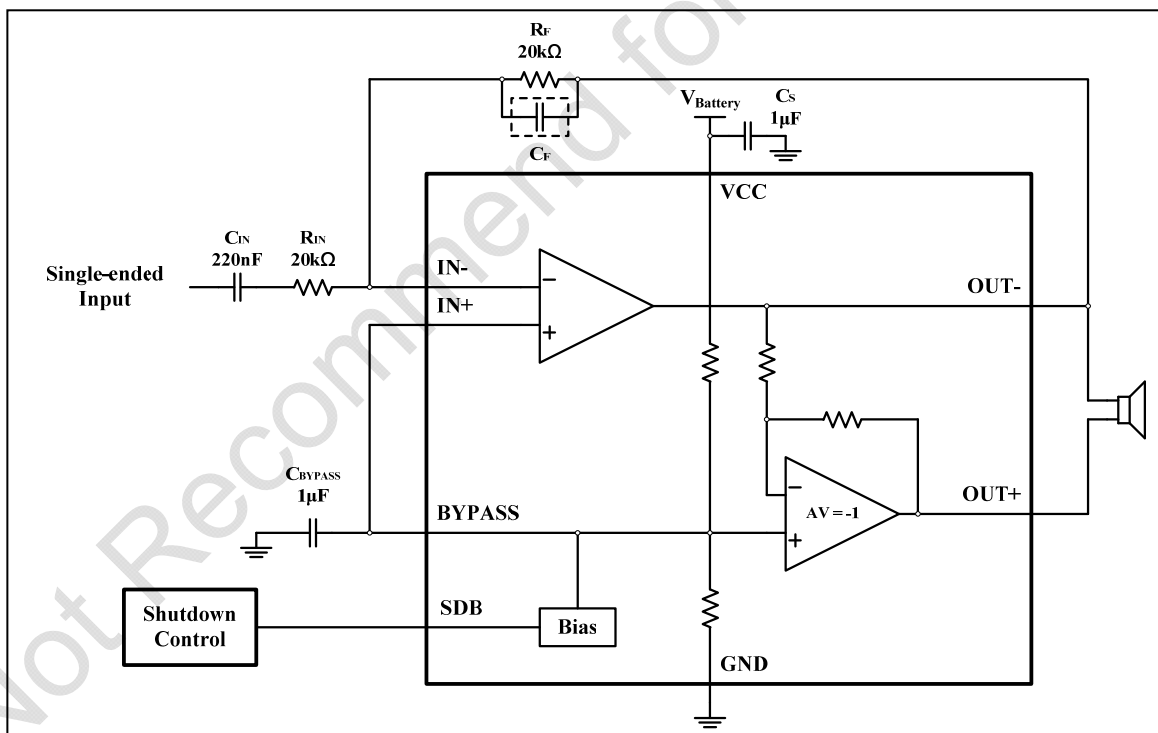


Figure 1 Typical Application Circuit (Single-ended input)

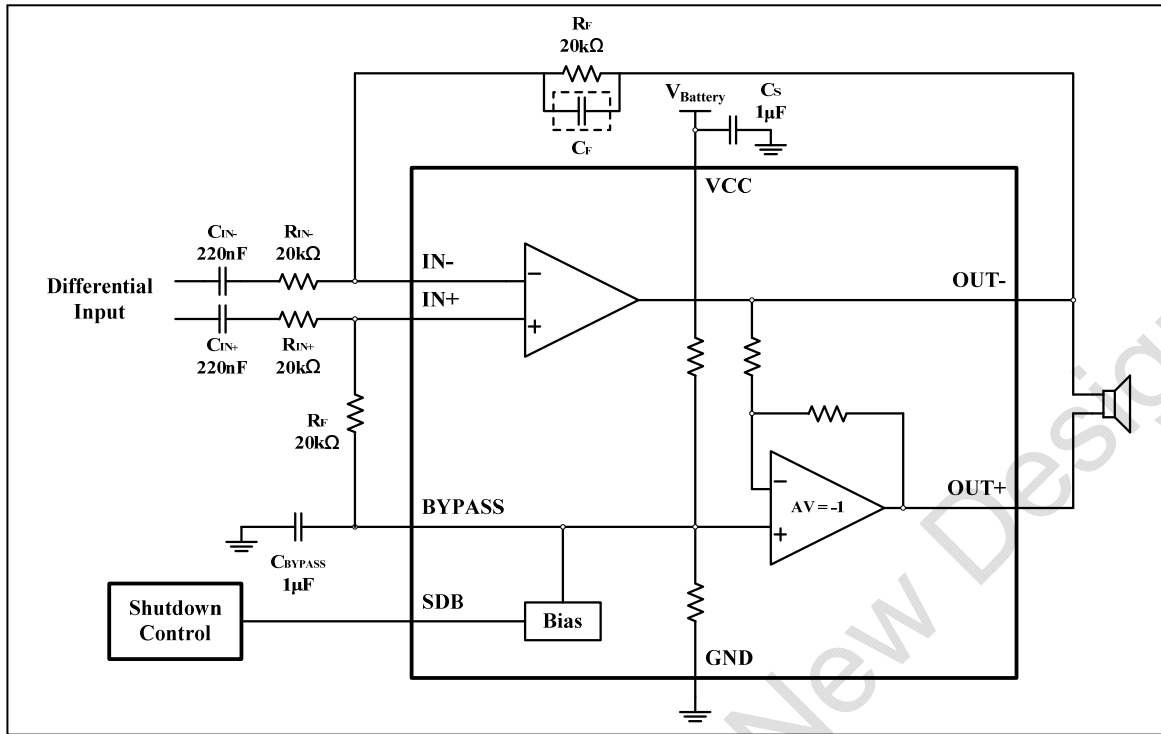
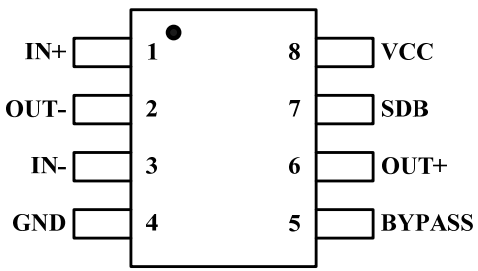
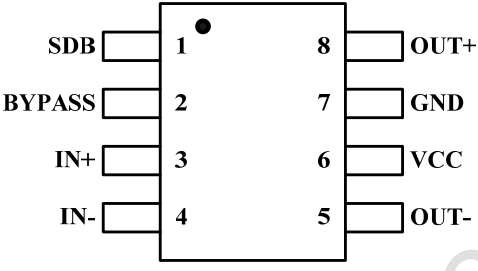


Figure 2 Typical Application Circuit (Differential input)

IS31AP4991

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP-8	
MSOP-8	

PIN DESCRIPTION

Pin	No.		Description
	SOP	MSOP	
IN+	1	3	Positive input of the first amplifier.
OUT-	2	5	Negative output of the IS31AP4991. Connected to the load and to the feedback resistor R_F .
IN-	3	4	Negative input of the first amplifier, receives the audio input signal. Connected to the feedback resistor R_F and to the input resistor R_{IN} .
GND	4	7	Ground.
BYPASS	5	2	Bypass capacitor pin which provides the common mode voltage ($V_{CC}/2$).
OUT+	6	8	Positive output of the IS31AP4991. Connected to the load.
SDB	7	1	The device enters shutdown mode when a low level is applied on this pin.
VCC	8	6	Positive analog supply of the chip.

IS31AP4991

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4991-GRLS2-TR	SOP-8, Lead-free	2500
IS31AP4991-SLS2-TR	MSOP-8, Lead-free	2500

Copyright © 2021 Lumissil Microsystems. All rights reserved. Lumissil Microsystems reserves the right to make changes to this specification and its products at any time without notice. Lumissil Microsystems assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

Lumissil Microsystems does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Lumissil Microsystems receives written assurance to its satisfaction, that:

- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

IS31AP4991

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{CC}+0.3V$
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for $C_{IN} = 0.22\mu F$, $R_{IN} = R_F = 20k\Omega$, $C_{BYPASS} = 1\mu F$, unless otherwise specified. Limits apply for $T_A = 25^\circ C$. $V_{CC}=5V$ (Note 2 or specified)

Symbol	Parameter	Condition	Typ.	Limit	Unit
I_{CC}	Quiescent power supply current	$V_{CC} = 0V$, $I_o = 0A$, no Load	4.8		mA (max)
I_{STBY}	Standby current	$V_{STBY} = GND$, $R_L = \infty$		1	μA (max)
V_{STBYH}	Shutdown voltage input high	$V_{CC} = 5.5V$		1.4	V(min)
V_{STBYL}	Shutdown voltage input low	$V_{CC} = 2.7V$		0.4	V(max)
V_{OS}	Output offset voltage			15	mV (max)
P_o	Output power (8 Ω)	THD+N = 1%; f = 1kHz	1.18		W
		THD+N = 10%; f = 1kHz	1.46		
t_{WU}	Wake-up time (Note 3)	$C_{BYPASS} = 1\mu F$	115		ms
THD+N	Total harmonic distortion+noise (Note 3)	$P_o = 0.5W_{rms}$; f = 1kHz	0.025		%
PSRR	Power supply rejection ratio (Note 3)	Vripple p-p = 200mV Input Grounded	f = 217Hz	65	dB
			f = 1kHz	77	

The following specifications apply for $C_{IN} = 0.22\mu F$, $R_{IN} = R_F = 20k\Omega$, $C_{BYPASS} = 1\mu F$, unless otherwise specified. Limits apply for $T_A = 25^\circ C$. $V_{CC}=3V$ (Note 2 or specified)

Symbol	Parameter	Condition	Typ.	Limit	Unit
I_{CC}	Quiescent power supply current	$V_{CC} = 0V$, $I_o = 0A$, no Load	3.8		mA(max)
I_{STBY}	Standby current	$V_{STBY} = GND$, $R_L = \infty$		1	μA (max)
P_o	Output power (8 Ω)	THD+N = 1%; f = 1kHz	405		mW
		THD+N = 10%; f = 1kHz	502		
t_{WU}	Wake-up time (Note 3)	$C_{BYPASS} = 1\mu F$	102		ms
THD+N	Total harmonic distortion+noise (Note 3)	$P_o = 0.3W_{rms}$; f = 1kHz	0.027		%

Note 2: Production testing of the device is performed at 25°C. Functional operation of the device and parameters specified over other temperature range, are guaranteed by design, characterization and process control.

Note 3: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTIC

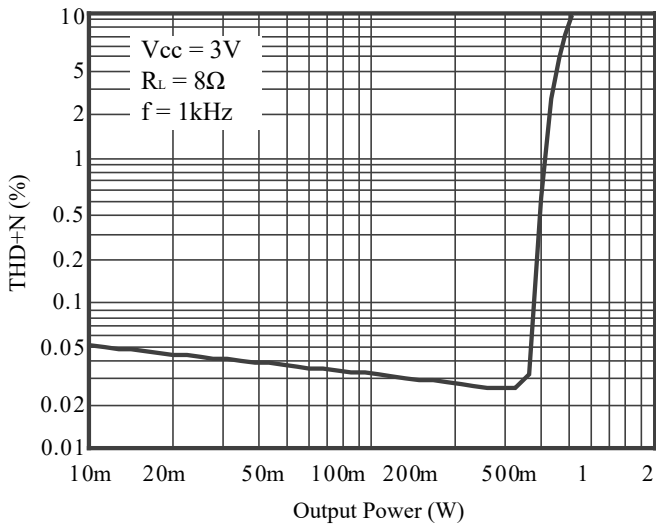


Figure 3 THD+N vs. Output Power

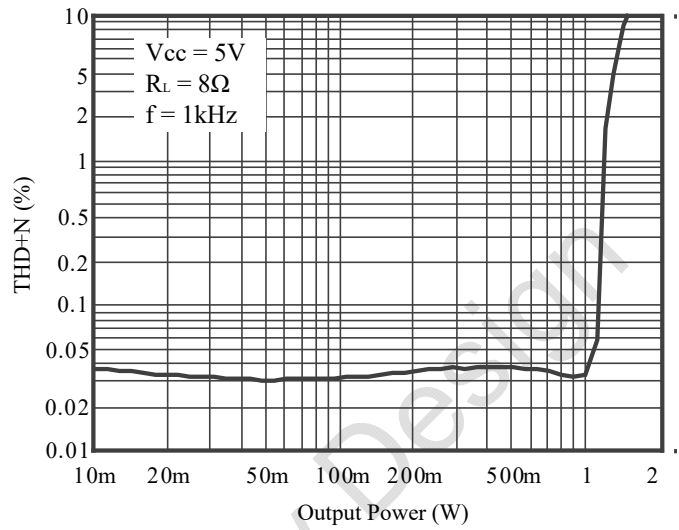


Figure 4 THD+N vs. Output Power

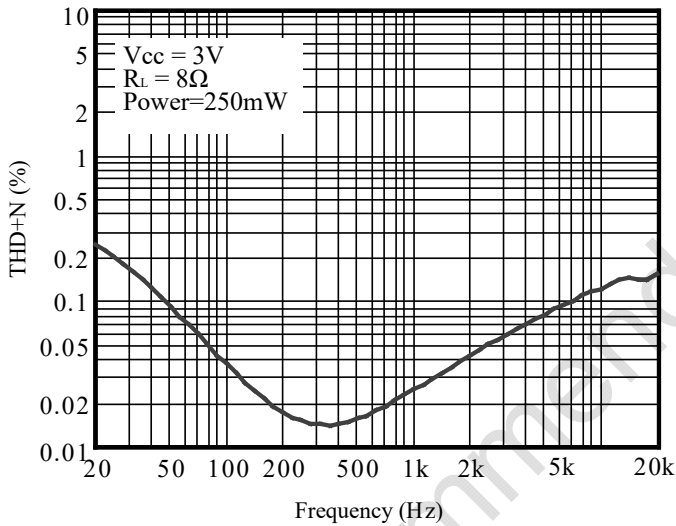


Figure 5 THD+N vs. Frequency

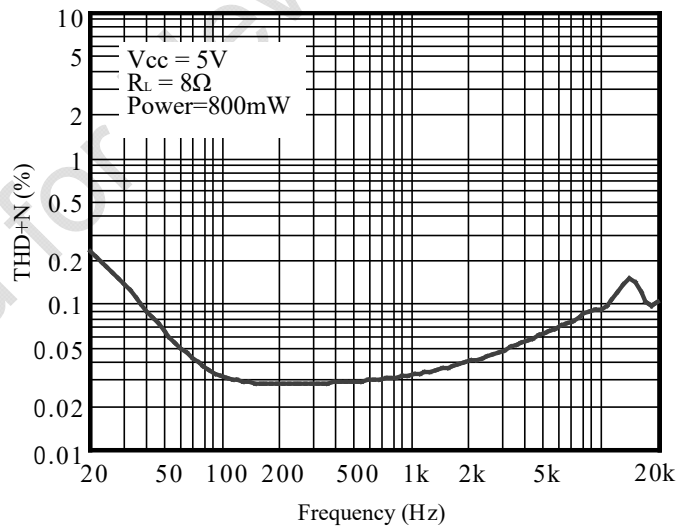


Figure 6 THD+N vs. Frequency

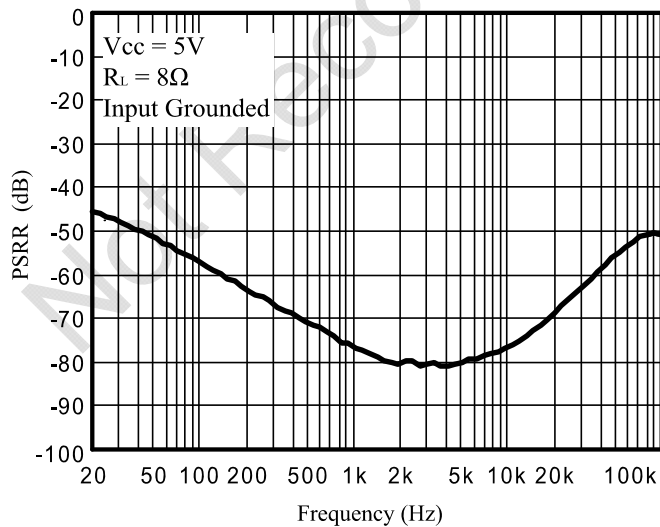


Figure 7 PSRR vs. Frequency

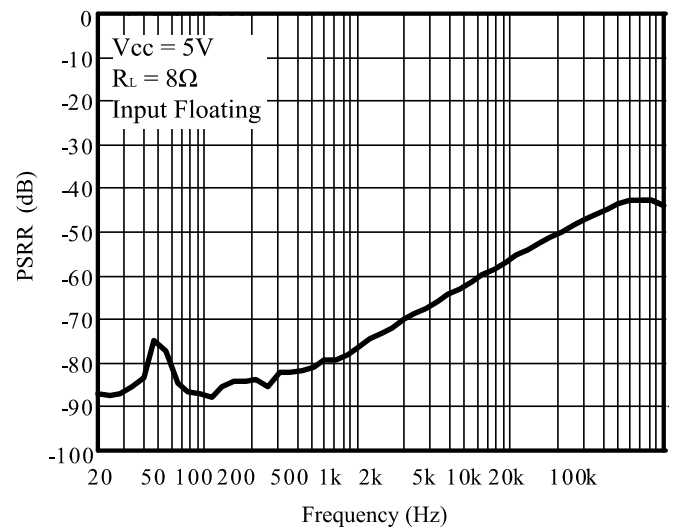


Figure 8 PSRR vs. Frequency

IS31AP4991

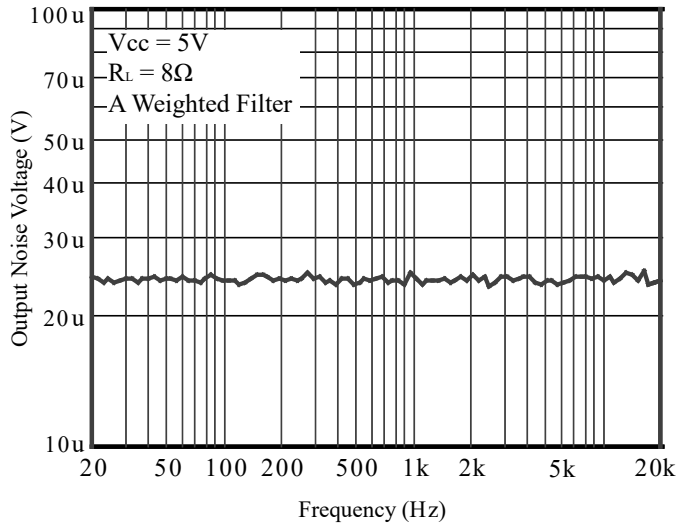


Figure 9 Noise Floor

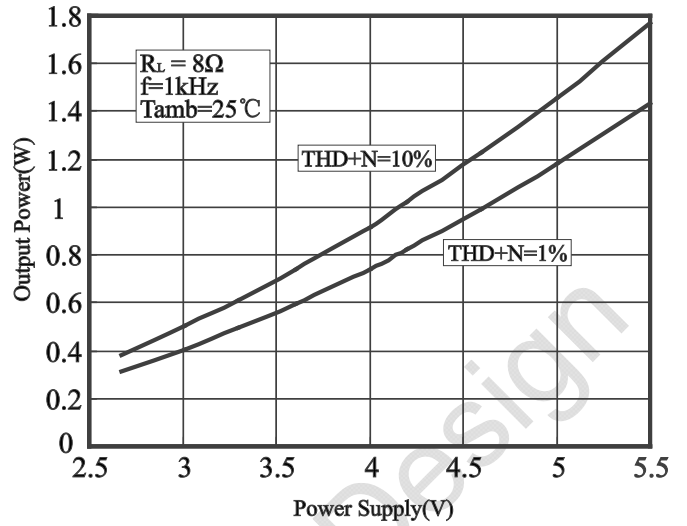


Figure 10 Output Power vs. Power Supply

IS31AP4991

APPLICATION INFORMATION

BTL CONFIGURATION PRINCIPLE

The IS31AP4991 is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single-ended output 1 = $V_{OUT+} = V_{OUT}$ (V)

Single ended output 2 = $V_{OUT-} = -V_{OUT}$ (V)

and

$V_{OUT+} - V_{OUT-} = 2V_{OUT}$ (V)

The output power is:

$$P_{OUT} = \frac{(2V_{OUT_{RMS}})^2}{R_L}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

GAIN IN A TYPICAL APPLICATION SCHEMATIC

The typical application schematic is shown in Figure 1 on page 1.

In the flat region (no C_{IN} effect), the output voltage of the first stage is (in Volts):

$$V_{OUT-} = (-V_{IN}) \frac{R_F}{R_{IN}}$$

For the second stage: $V_{OUT+} = -V_{OUT-}$ (V)

The differential output voltage is (in Volts):

$$V_{OUT+} - V_{OUT-} = 2V_{IN} \frac{R_F}{R_{IN}}$$

The differential gain, G_v , is given by:

$$G_v = \frac{V_{OUT+} - V_{OUT-}}{V_{IN}} = 2 \frac{R_F}{R_{IN}}$$

V_{OUT-} is in phase with V_{IN} and V_{OUT+} is phased 180° with V_{IN} . This means that the positive terminal of the loudspeaker should be connected to V_{OUT+} and the negative to V_{OUT-} .

LOW AND HIGH FREQUENCY RESPONSE

In the low frequency region, C_{IN} starts to have an effect. C_{IN} forms with R_{IN} a high-pass filter with a -3dB cut-off frequency. f_{CL} is in Hz.

$$f_{CL} = \frac{1}{2\pi R_{IN} C_{IN}}$$

In the high frequency region, you can limit the bandwidth by adding a capacitor (C_F) in parallel with R_F . It forms a low-pass filter with a -3dB cut-off frequency.

f_{CH} is in Hz.

$$f_{CH} = \frac{1}{2\pi R_F C_F}$$

DECOUPLING OF THE CIRCUIT

Two capacitors are needed to correctly bypass the IS31AP4991: a power supply bypass capacitor C_S and a bias voltage bypass capacitor C_{BYPASS} .

C_S has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_S of $1\mu F$, you can expect THD+N levels similar to those shown in the datasheet.

In the high frequency region, if C_S is lower than $1\mu F$, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is higher than $1\mu F$, those disturbances on the power supply rail are more filtered.

C_{BYPASS} has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_{BYPASS} is lower than $1\mu F$, THD+N increases at lower frequencies and PSRR worsens.

If C_{BYPASS} is higher than $1\mu F$, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that C_{IN} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{IN} , the higher the PSRR is.

WAKE-UP TIME (t_{WU})

When the standby is released to put the device on, the bypass capacitor C_{BYPASS} will not be charged immediately. As C_{BYPASS} is directly linked to the bias of the amplifier, the bias will not work properly until the C_{BYPASS} voltage is correct. The time to reach this voltage is called wake-up time or t_{WU} and specified in the electrical characteristics table with $C_{BYPASS} = 1\mu F$.

POP PERFORMANCE

Pop performance is intimately linked with the size of the input capacitor C_{IN} and the bias voltage bypass capacitor C_{BYPASS} .

The size of C_{IN} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_{BYPASS} is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_{BYPASS} determines the speed with which the amplifier turns on.

IS31AP4991

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak	
Temperature min (T _{smIn})	150°C
Temperature max (T _{smax})	200°C
Time (T _{smIn} to T _{smax}) (t _s)	60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L)	217°C
Time at liquidous (t _L)	60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

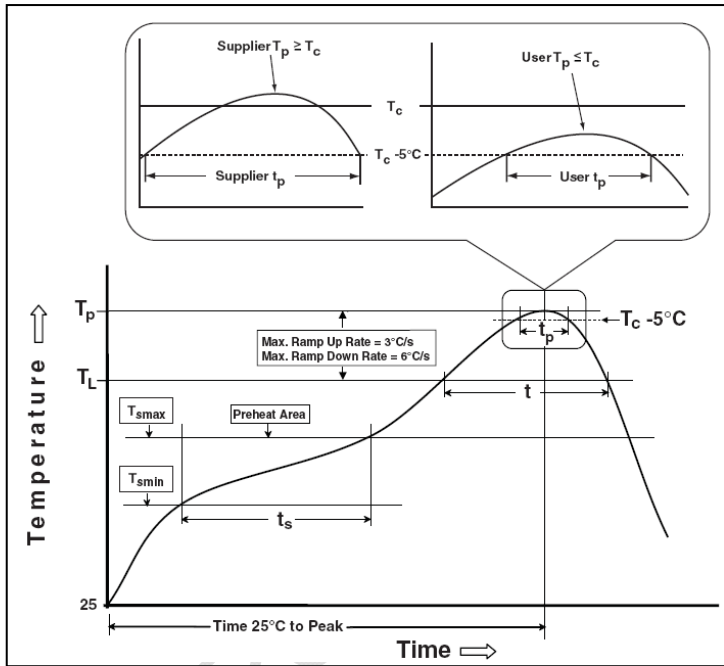
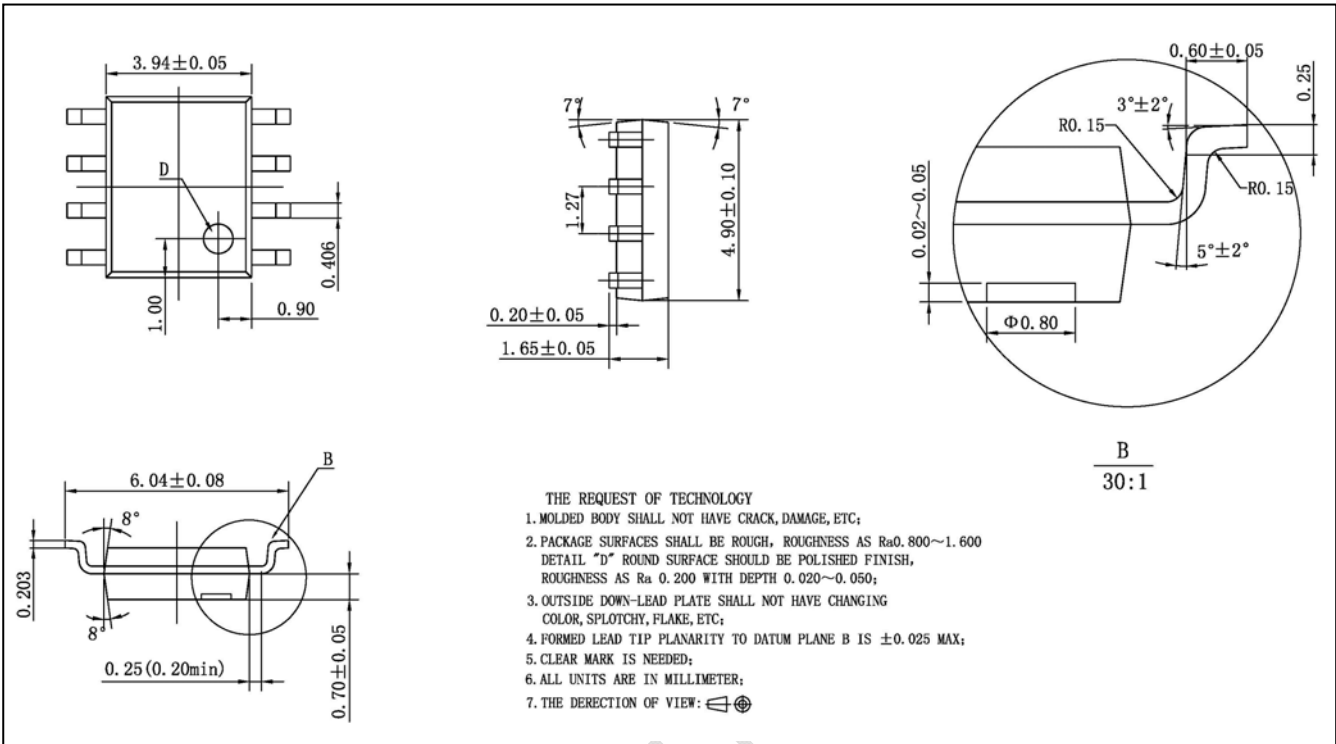


Figure 11 Classification Profile

IS31AP4991

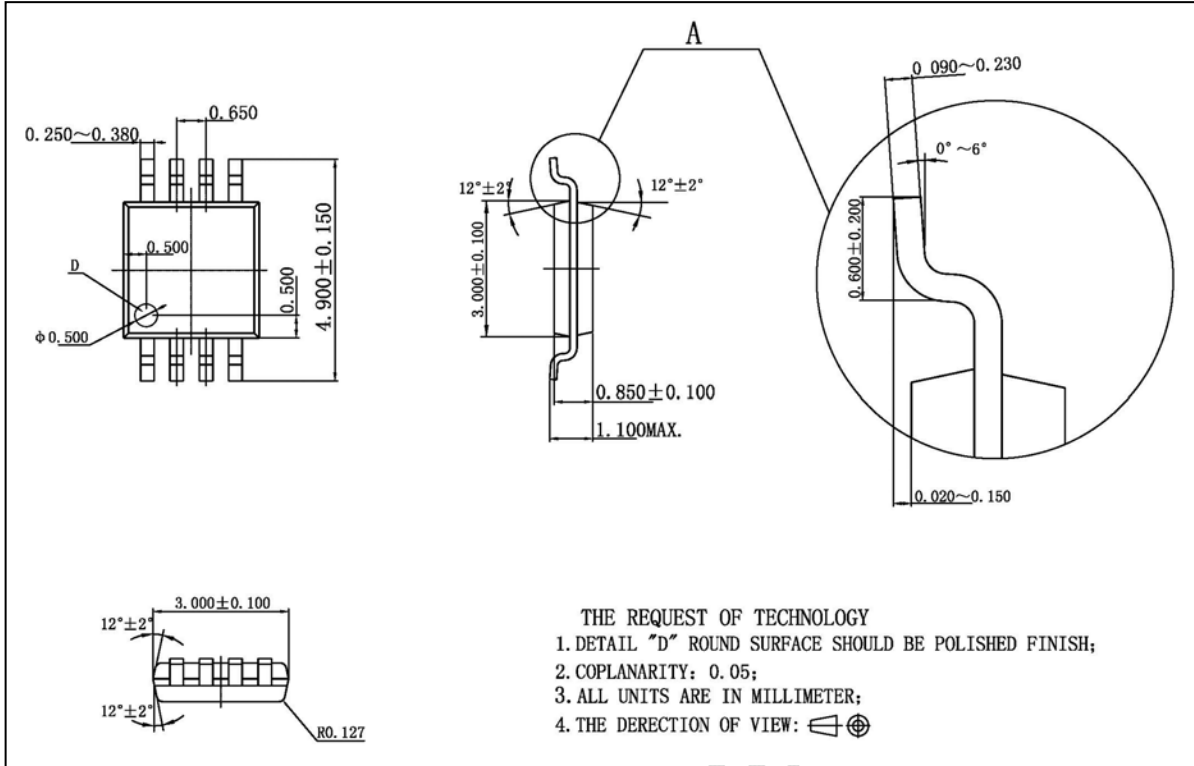
PACKAGE INFORMATION

SOP-8



IS31AP4991

MSOP-8



REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.11.25
B	1. P.2 Add differential input circuit 2. P.10 Delete tape and reel information	2012.10.23
C	Add NRND watermark	2021.09.07

Not Recommend for New Design