| PCN Number: | 20110221003C | PCN Date: | 09/10/2013 |
|---|---|---|---|
| Title: | Qualification of TSMC-WF9 as an additional wafer fab site for select devices in the 0.35um DPTM and DPQM process technologies | | |
| Customer Contact: | PCN Manager | Phone: +1(214)480-6037 | Dept: Quality Services |

**Change Type:**

| | | | | | |
|---|---|---|---|---|---|
| ☐ | Assembly Site | ☐ | Assembly Process | ☐ | Assembly Materials |
| ☐ | Design | ☐ | Electrical Specification | ☐ | Mechanical Specification |
| ☐ | Test Site | ☐ | Packing/Shipping/Labeling | ☐ | Test Process |
| ☐ | Wafer Bump Site | ☐ | Wafer Bump Material | ☐ | Wafer Bump Process |
| ☒ | Wafer Fab Site | ☐ | Wafer Fab Materials | ☐ | Wafer Fab Process |

## PCN Details

**Description of Change:**

**Revision C** is to announce the retraction of select devices. These will continue to be sourced from their current location, TSMC-WF3. Affected devices are identified with a **~~strikethrough~~** and are highlighted in yellow in the Product Affected Section, Group B.

Revision A is to announce the qualification of TSMC-WF9 as an additional wafer fab site for the select devices in the 0.35um DPTM and DPQM process technologies currently sourced at TSMC WF3.

**Device Groupings in the Product Affection Section:**

**Group A: Devices Released Rev A (Issued 2/27/2012)**
**Group B: Devices Retracted Rev B (Issued 7/06/2012)**
**Group C: Devices Being Retracted This Rev C (9/09/2013)**

The 0.35 DPTM process was previously qualified at TSMC FAB-WF9 on 07/21/2006. Qual details are provided in the Qual Data Section

**Reason for Change:**

Continuity of supply.

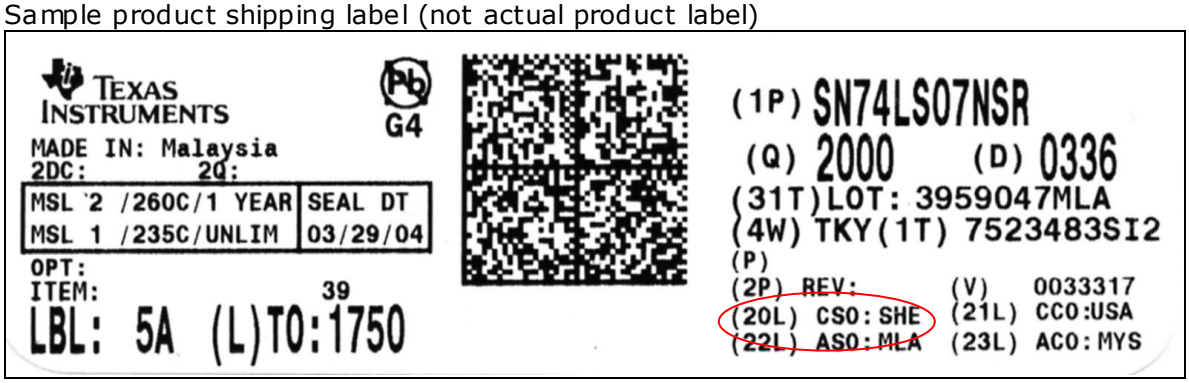
**Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):**

None.

**Changes to product identification resulting from this PCN:**

| | Chip Site | Chip site code (20L) |
|---|---|---|
| Current | TSMC-WF3 | CSO:TS5 |
| **New** | **TSMC-WF9** | **CSO:TS9** |

Sample product shipping label (not actual product label)



## Product Affected:

| Group A: Device Qualified/Released Rev A (Issued 2/27/2012) | | | |
|---|---|---|---|
| HPA00026DBR | PCM1802DBRG4 | PCM2704DBRG4 | PCM2705DBG4 |
| PCM1802DB | PCM2704DB | PCM2704S1DB | PCM2705DBR |
| PCM1802DBG4 | PCM2704DBG4 | PCM2704S1DBR | PCM2705DBRG4 |
| PCM1802DBR | PCM2704DBR | PCM2705DB | |
| | | | |
| **Group B: Devices Retracted in Rev B (Issued 7/06/2012)** | | | |
| ~~DIX9211PT~~ | ~~PCM1782DBQG4~~ | ~~PCM2900E-P~~ | ~~PCM2902EG4~~ |
| ~~DIX9211PTR~~ | ~~PCM1782DBQR~~ | ~~PCM2900E-PG4~~ | ~~PCM2903E~~ |
| ~~HPA00419RGPR~~ | ~~PCM1782DBQRG4~~ | ~~PCM2901E~~ | ~~PCM2903E/2K~~ |
| ~~HPA00436E/2K~~ | ~~PCM2900E~~ | ~~PCM2901E/2K~~ | ~~PCM2903E/2KG4~~ |
| ~~PCM1774RGPR~~ | ~~PCM2900E/2K~~ | ~~PCM2901E/2KG4~~ | ~~PCM2903EG4~~ |
| ~~PCM1774RGPRG4~~ | ~~PCM2900E/2KG4~~ | ~~PCM2901EG4~~ | ~~PCM9211PT~~ |
| ~~PCM1774RGPT~~ | ~~PCM2900EG/2K~~ | ~~PCM2902E~~ | ~~PCM9211PTR~~ |
| ~~PCM1774RGPTG4~~ | ~~PCM2900EG/2KE6~~ | ~~PCM2902E/2K~~ | |
| ~~PCM1782DBQ~~ | ~~PCM2900EG4~~ | ~~PCM2902E/2KG4~~ | |
| | | | |
| **Group C: Devices Retracted This Rev C (9/09/2013)** | | | |
| ~~**PCM1681PWP**~~ | ~~**PCM1681PWPG4**~~ | ~~**PCM1681PWPR**~~ | ~~**PCM1681PWPRG4**~~ |

## Qualification Data:

This qualification has been specifically developed for the validation of this change. The qualification data validates that the proposed change meets the applicable released technical specifications.

| **Qualification Schedule:** | **Start:** | 05/2011 | **End:** | ~~11/30/2012~~ |
|---|---|---|---|---|

**Qual Vehicle 1: PCM1802DB (Approved: 5/12/2011)**

**Die Construction Details**

| Wafer Fab Site: | TSMC FAB9 | Metallization 1: | AlCu |
|---|---|---|---|
| Wafer Fab Process: | 0.35 DPTM | Passivation: | SiO2 ; SOG ; Si3N4 |

**Qualification:** ☐ **Plan** ☒ **Test Results**

| Reliability Test | Conditions | # Lots | SS/Lot | Fails |
|---|---|---|---|---|
| Electrical Characterization | Full Temp & Voltage range | 1 | Pass | 0 |
| Manufacturability (Wafer Fab) | Per mfg. Site specification | 1 | Approved | - |

**Qual Vehicle 2: PCM2705DB (Approved: 1/13/2012)**

**Package / Die Construction Details**

| Wafer Fab Site: | TSMC FAB9 | Metallization 1: | AlCu |
|---|---|---|---|
| Wafer Fab Process: | 0.35 DPTM | Passivation: | SiO2 ; SOG ; Si3N4 |

**Qualification:** ☐ **Plan** ☒ **Test Results**

| Reliability Test | Conditions | # Lots | SS/Lot | Fails |
|---|---|---|---|---|
| Electrical Characterization | Full Temp & Voltage range | 1 | Pass | 0 |
| Manufacturability (Wafer Fab) | Per mfg. Site specification | 1 | Approved | - |

| ~~Qual Vehicle 3: PCM1681PWPR~~ | | | | |
|---|---|---|---|---|
| **Package / Die Construction Details** | | | | |
| Wafer Fab Site: | TSMC FAB9 | Metallization 1: | AlCu | |
| Wafer Fab Process: | 0.35 DPQM | | | |
| **Qualification:** ☒ **Plan** ☐ **Test Results** | | | | |
| Reliability Test | Conditions | # Lots | SS/Lot | Fails |
| Electrical Characterization | Full Temp & Voltage range | 1 | 30 | 0 |
| **Autoclave 121C | 121C, 2 atm (96 Hrs) | 3 | 77 | 0 |
| **T/C -65C/150C | -65C/+150C (500 Cyc) | 3 | 77 | 0 |
| ESD CDM | 500V | 1 | 3 | 0 |
| ESD HBM | 2000V | 1 | 3 | 0 |
| Ball Bond Shear | 76 balls, 3 units min | 3 | 76 | 0 |
| Bond Pull | 76 Wire, 3 units min | 3 | 76 | 0 |
| Wafer level Reliability | Per Site Specification | 3 | Pass | - |
| Latch-up | ( per JESD78 ) | 1 | 6 | 0 |
| Manufacturability (Assembly) | (per mfg. Site specification) | 3 | Pass | - |
| Manufacturability (Wafer Fab) | (per mfg. Site specification) | 3 | Pass | - |
| ** Preconditioning: level 3 @ 260C | | | | |

| ~~Qual Vehicle 4: PCM1774RGPR~~ | | | | |
|---|---|---|---|---|
| **Package / Die Construction Details** | | | | |
| Wafer Fab Site: | TSMC FAB9 | Metallization 1: | AlCu | |
| Wafer Fab Process: | 0.35 DPQM | | | |
| **Qualification:** ☒ **Plan** ☐ **Test Results** | | | | |
| Reliability Test | Conditions | # Lots | SS/Lot | Fails |
| Electrical Characterization | Full Temp & Voltage range | 1 | 30 | 0 |
| ESD CDM | 500V | 1 | 3 | 0 |
| ESD HBM | 2000V | 1 | 3 | 0 |
| Wafer level Reliability | Per Site Specification | 1 | Pass | - |
| Latch-up | ( per JESD78 ) | 1 | 6 | 0 |
| Manufacturability (Assembly) | (per mfg. Site specification) | 1 | Pass | - |
| Manufacturability (Wafer Fab) | (per mfg. Site specification) | 1 | Pass | - |

| ~~Qual Vehicle 5: PCM1782DBQR~~ | | | | |
|---|---|---|---|---|
| **Package / Die Construction Details** | | | | |
| Wafer Fab Site: | TSMC FAB9 | Metallization 1: | AlCu | |
| Wafer Fab Process: | 0.35 DPQM | | | |
| **Qualification:** ☒ **Plan** ☐ **Test Results** | | | | |
| Reliability Test | Conditions | # Lots | SS/Lot | Fails |
| Electrical Characterization | Full Temp & Voltage range | 1 | 30 | 0 |
| Manufacturability (Wafer Fab) | (per mfg. Site specification) | 1 | Pass | - |

| ~~Qual Vehicle 6: PCM9211PTR~~ | | | | |
|---|---|---|---|---|
| **Package / Die Construction Details** | | | | |
| Wafer Fab Site: | TSMC FAB9 | Metallization 1: | AlCu | |
| Wafer Fab Process: | 0.35 DPQM | | | |
| **Qualification:** ☒ **Plan** ☐ **Test Results** | | | | |
| Reliability Test | Conditions | # Lots | SS/Lot | Fails |
| Electrical Characterization | Full Temp & Voltage range | 1 | 30 | 0 |
| Manufacturability (Wafer Fab) | (per mfg. Site specification) | 1 | Pass | - |

## 0.35 DPTM Process Qualification Data: (Approved 07/21/2006)

This qualification has been specifically developed for the validation of this change. The qualification data validates that the proposed change meets the applicable released technical specifications.

| Qual Vehicle 1 : PCM1802DB | | | | |
|---|---|---|---|---|
| **Package / Die Construction Details** | | | | |
| Wafer Fab Site: | TSMC-FAB9 | Metallization: | Al-Si-Cu | |
| Wafer Fab Process: | 0.35um DPTM Dual gate | Passivation: | SiO2 /SiN 1.5/10kA | |
| **Qualification:** ☐ **Plan** ☒ **Test Results** | | | | |
| Reliability Test | Conditions | # Lots | SS/Lot | Fails |
| **High Temp Operating Life | 125C (1000 Hrs) | 1 | 120 | 0 |
| **T/C -65C/150C | -65C/+150C (500 Cycles) | 1 | 81 | 0 |
| **High Temp Storage Life | 170C (420 Hrs) | 1 | 81 | 0 |
| **Thermal Shock | -65C/+150C (500 Cycles) | 1 | 81 | 0 |
| **Biased HAST | 130C/85%RH (96 Hrs) | 1 | 80 | 0 |
| **Autoclave 121C | 121C, 2Atm (96 Hrs) | 1 | 80 | 0 |
| ESD HBM (3 units/voltage) | 1500V | 1 | 3 | 0 |
| ESD CDM (3 units/voltage) | 1000V | 1 | 3 | 0 |
| Latch-up | (per JESD78) | 1 | 6 | 0 |
| **- Preconditioning Sequence: L1-260C | | | | |

| Qual Vehicle 2 : PCM1807PW | | | | | |
|---|---|---|---|---|---|
| **Package / Die Construction Details** | | | | | |
| Wafer Fab Site: | TSMC-FAB9 | | Metallization: | Al-Si-Cu | |
| Wafer Fab Process: | 0.35um DPTM Dual gate | | Passivation: | SiO2 /SiN 1.5/10kA | |
| **Qualification:** ☐ **Plan** ☒ **Test Results** | | | | | |
| Reliability Test | Conditions | | # Lots | SS/Lot | Fails |
| **High Temp Operating Life | 125C (1000 Hrs) | | 2 | 120 | 0 |
| **T/C -65C/150C | -65C/+150C (500 Cycles) | | 2 | 84 | 0 |
| **High Temp Storage Life | 170C (420 Hrs) | | 2 | 80 | 0 |
| **Thermal Shock | -65C/+150C (500 Cycles) | | 2 | 80 | 0 |
| **Biased HAST | 130C/85%RH (96 Hrs) | | 2 | 80 | 0 |
| **Autoclave 121C | 121C, 2Atm (96 Hrs) | | 2 | 80 | 0 |
| ESD HBM (3 units/voltage) | 2000V | | 2 | 3 | 0 |
| ESD CDM (3 units/voltage) | 1000V | | 2 | 3 | 0 |
| Latch-up | (per JESD78) | | 2 | 6 | 0 |
| **- Preconditioning Sequence: L1-260C | | | | | |

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

| Location | E-Mail |
|---|---|
| USA | PCNAmericasContact@list.ti.com |
| Europe | PCNEuropeContact@list.ti.com |
| Asia Pacific | PCNAsiaContact@list.ti.com |
| Japan | PCNJapanContact@list.ti.com |