

# High Power Switch - LNA Module

## 0.4 - 5.0 GHz



MAIA-011004

Rev. V3

### Features

- 2-Stage LNA and High Power Switch
- High RF Input Power:
  - 120 W CW @ +85°C, 2.0 GHz
  - 100 W CW @ +85°C, 2.7 GHz
- Noise Figure:
  - 0.85 dB @ 2.0 GHz
  - 1.0 dB @ 2.7 GHz
- Gain:
  - 37 dB @ 2.0 GHz
  - 34 dB @ 2.7 GHz
- OIP3: 36 dBm
- Lead-Free 5 mm 32-lead HQFN
- Integrated ESD Protection
- Halogen-Free “Green” Mold Compound
- ROHS\* Compliant

### Description

The MAIA-011004 is a compact surface mount module containing a PIN diode switch and two low noise amplifiers assembled in a 5 mm 32-lead HQFN plastic package. It was designed to be used at the input of the receive chain of TDD cellular base stations.

This module operates from 0.4 GHz to 5.0 GHz and features high power handling, very low noise figure and excellent linearity.

The connection between the output of LNA1 and the input of LNA2 is made outside of the module, making it possible for the user to add an attenuator or a filter.

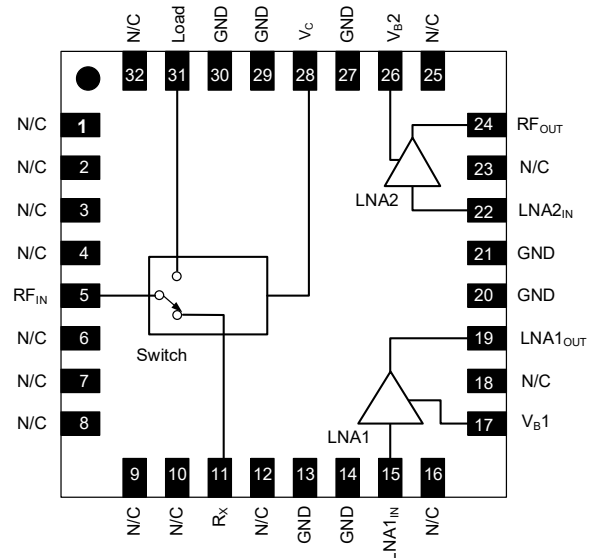
The MAIA-011004 is ideally suited for 4G and next generation 5G base stations at 1.9, 2.3, 2.6, 3.5, and 4.5 GHz.

### Ordering Information<sup>1,2</sup>

Part Number	Package
MAIA-011004-TR1000	1k Piece Reel
MAIA-011004-TR3000	3k Piece Reel
MAIA-011004-1SMB	2 - 3 GHz Sample Board
MAIA-011004-2SMB	3 - 4 GHz Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

### Functional Schematic



### Pin Configuration

Pin #	Pin Name	Function
1-4, 6-10, 12, 16, 18, 23, 25, 32	N/C <sup>3</sup>	No Connection
5	RF <sub>IN</sub>	RF Input / Bias
11	R <sub>X</sub>	R <sub>X</sub> Switch Output
13, 14, 20, 21, 27, 29, 30	GND	RF Ground
15	LNA1 <sub>IN</sub>	LNA1 Input
17	V <sub>B1</sub>	LNA1 Bias
19	LNA1 <sub>OUT</sub>	LNA1 Output / V <sub>DD1</sub>
22	LNA2 <sub>IN</sub>	LNA2 Input
24	RF <sub>OUT</sub>	RF Output / V <sub>DD2</sub>
26	V <sub>B2</sub>	LNA2 Bias
28	V <sub>C</sub>	Switch Bias Control
31	Load	T <sub>X</sub> Switch Output
33	Paddle	Ground <sup>4</sup>

3. MACOM recommends connecting unused package pins (N/C) to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

\* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

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### Electrical Specifications<sup>5</sup>:

$T_A = +25^\circ\text{C}$ ,  $V_{DD1} = 3\text{ V}$ ,  $V_{BB1} = 3\text{ V}$ ,  $V_{DD2} = 3\text{ V}$ ,  $V_{BB2} = 3\text{ V}$

Switch Bias = (see Bias Table),  $R_{BIAS2} = 133\ \Omega$ ,  $R_{BIAS1} = 100\ \Omega$ ,  $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Input RF Power @ +85°C RF <sub>IN</sub> - LOAD	2.0 GHz 2.7 GHz 3.5 GHz	W	—	120 100 80	—
Insertion Loss RF <sub>IN</sub> - LOAD	2.0 GHz 2.7 GHz 3.5 GHz	dB	—	0.15 0.18 0.21	—
Noise Figure RF <sub>IN</sub> - RF <sub>OUT</sub>	2.0 GHz 2.7 GHz 3.5 GHz	dB	—	0.85 1.00 1.25	—
Gain RF <sub>IN</sub> - RF <sub>OUT</sub>	2.0 GHz 2.7 GHz 3.5 GHz	dB	—	37 34 32	—
Isolation RF <sub>IN</sub> - LNA1 <sub>IN</sub>	Switch State = RF <sub>IN</sub> - LOAD 2.7 GHz	dB	—	41	—
Isolation LNA1 <sub>OUT</sub> - LNA2 <sub>IN</sub>	Switch State = RF <sub>IN</sub> - RF <sub>OUT</sub> 2.7 GHz	dB	—	40	—
Output IP3 RF <sub>IN</sub> - RF <sub>OUT</sub>	P <sub>IN</sub> = -35 dBm, Tones 11 MHz apart 2.7 GHz	dBm	—	36	—
LNA Bias Current	LNA1 Current: I <sub>DD1</sub> + I <sub>V<sub>B</sub>1</sub> LNA2 Current: I <sub>DD2</sub> + I <sub>V<sub>B</sub>2</sub>	mA	—	75 65	—

5. Refer to LNA biasing options on page 4.

### Switch Bias Table (See Sample Board Schematic on Page 9)

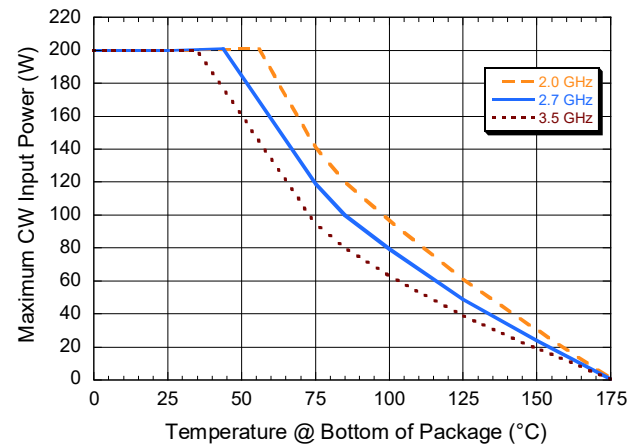
RF <sub>IN</sub> - LOAD	RF <sub>IN</sub> - RF <sub>OUT</sub>	LOAD_B	R <sub>x</sub> Bias	R <sub>x</sub> _ShD_B	V <sub>RF<sub>IN</sub></sub>
ON	OFF	0 V (-50 mA)	+28 V (50 mA)	0 V (-50 mA)	3 V (50 mA)
OFF	ON	+28 V (0 mA)	0 V (-50 mA)	+28 V (0 mA)	3 V (50 mA)

### Absolute Maximum Ratings<sup>6,7,8</sup>

Parameter	Absolute Maximum
RF Input Power RF <sub>IN</sub> - RF <sub>OUT</sub> RF <sub>IN</sub> - LOAD	19 dBm See Power De-rating Curve
Switch Reverse Voltage (RF & DC)	160 V
V <sub>B1</sub> & V <sub>B2</sub>	5.0 V
LNA1 <sub>OUT</sub> & RF <sub>OUT</sub>	5.5 V
Junction Temperature Switch LNA <sup>9</sup>	+175°C +150°C
Operating Temperature	-40°C to +100°C
Storage Temperature	-55°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Operating at nominal conditions with  $T_J \leq$  Absolute Maximum will ensure MTTF  $> 1 \times 10^6$  hours.
9. LNA Junction Temperature ( $T_J$ ) =  $T_C + \Theta_{JC} \cdot (V \cdot I)$   
 Typical thermal resistance ( $\Theta_{JC}$ ) = 83°C/W
  - a) For  $T_C = +25^\circ\text{C}$ ,  
 $T_J = 56^\circ\text{C}$  @  $V_{DD1} = 5\text{ V}$ , 75 mA for LNA1  
 $T_J = 52^\circ\text{C}$  @  $V_{DD2} = 5\text{ V}$ , 65 mA for LNA2
  - b) For  $T_C = +100^\circ\text{C}$ ,  
 $T_J = 131^\circ\text{C}$  @  $V_{DD1} = 5\text{ V}$ , 75 mA for LNA1  
 $T_J = 127^\circ\text{C}$  @  $V_{DD1} = 5\text{ V}$ , 65 mA for LNA2

### T<sub>x</sub> Input Power De-rating @ 20 dB I/O Return Loss



### Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Parameter	Rating	Standard
Human Body Model (HBM)	500 V (Class 1B)	ESDA / JEDEC JS-001
Charged Device Model (CDM)	1000 V (Class C3)	JEDEC JESD22-C101

### LNA Biasing Options

LNA1 and LNA2 biases can be set in 2 different ways: using only  $V_{DD}$ , or using separate  $V_{DD}$  and  $V_{BIAS}$  [ $V_B$ ] voltages. A separate  $V_{BIAS}$  voltage allows  $V_{B1}$  and  $V_{B2}$  to be used as enable pins to power LNA1 and LNA2 up and down during operation.

For both bias methods, select the value of  $R_{BIAS1}$  and  $R_{BIAS2}$  to achieve the desired currents using the plots on page 5. LNA1 current should not exceed 100 mA @ 25 °C and likewise LNA2 current should not exceed 95 mA @ 25 °C. DC blocking capacitors must be used at the LNA1 and 2 input and output ports (see diagram).

### Biasing Option - $V_{DD}$ only

To use only  $V_{DD}$ , connect to  $V_{DD}$  [1,2] through an RF inductor and connect  $V_B$  [1,2] to the corresponding  $V_{DD}$  through bias resistor  $R_{BIAS}$  [1,2] as shown in Figure 1.

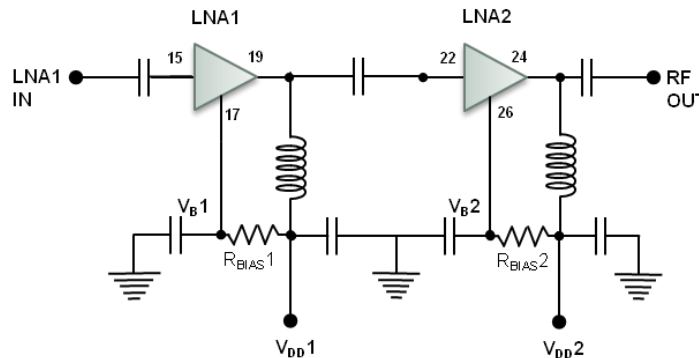


Figure 1

### Biasing Option - Separate $V_{DD}$ and $V_{BB}$ Voltages ( $V_{BB} \leq V_{DD}$ )

To use separate  $V_{DD}$  and  $V_{BB}$  voltages, connect to  $V_{DD}$  [1,2] through an RF inductor and connect to  $V_{BB}$  [1,2] through bias resistor  $R_{BIAS}$  [1,2] as shown in Figure 2. Typical current draw for  $V_B$  [1,2] is 1.4 mA @  $V_{BB} = 3$  V, and 1  $\mu$ A @  $V_{BB} = 0$  V. Typical current draw for  $V_{DD}$  [1,2] is < 1  $\mu$ A @  $V_{BB} = 0$  V and  $V_{DD} = 3$ V.

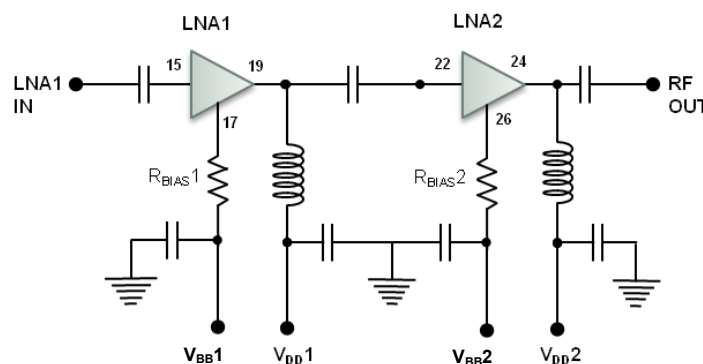
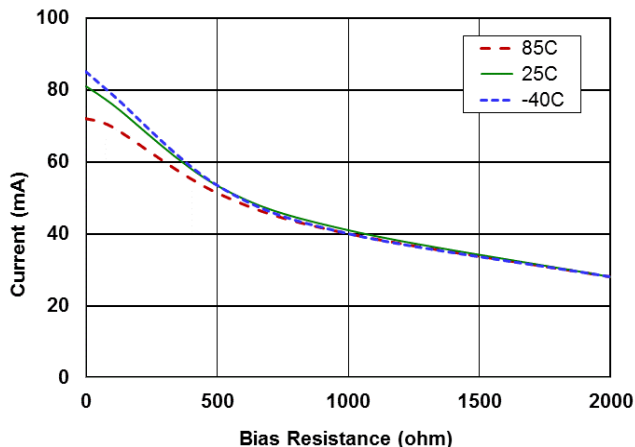


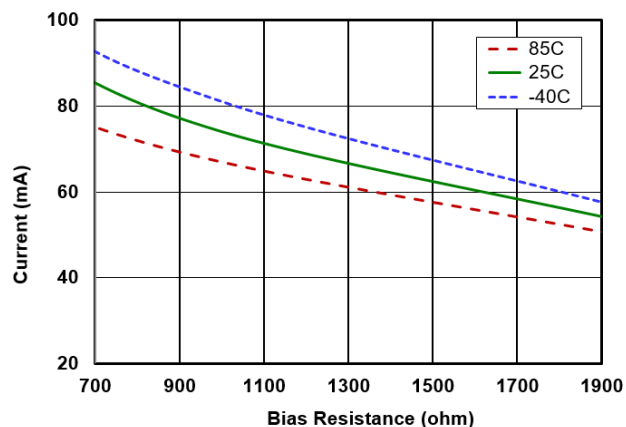
Figure 2

### Typical Performance Curves: LNA1 Bias Current over Temperature

LNA1 Current,  $V_{DD1} = 3\text{ V}$

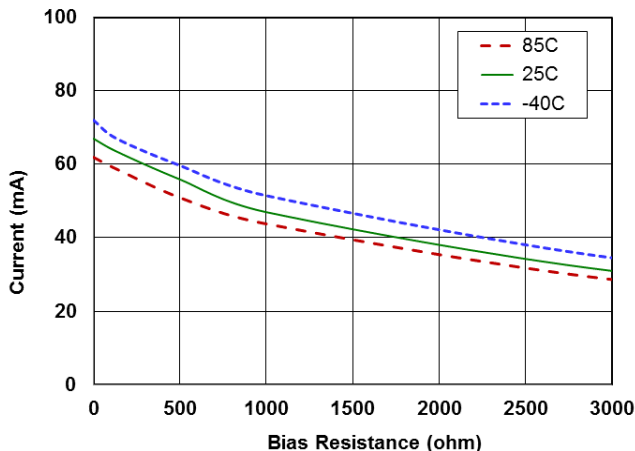


LNA1 Current,  $V_{DD1} = 5\text{ V}$

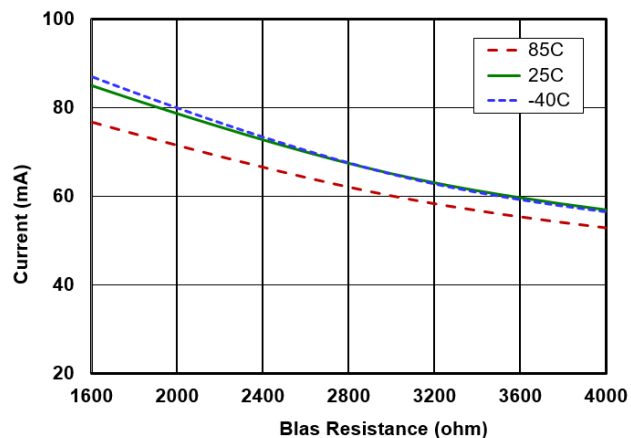


### Typical Performance Curves: LNA2 Bias Current over Temperature

LNA2 Current,  $V_{DD2} = 3\text{ V}$



LNA2 Current,  $V_{DD2} = 5\text{ V}$



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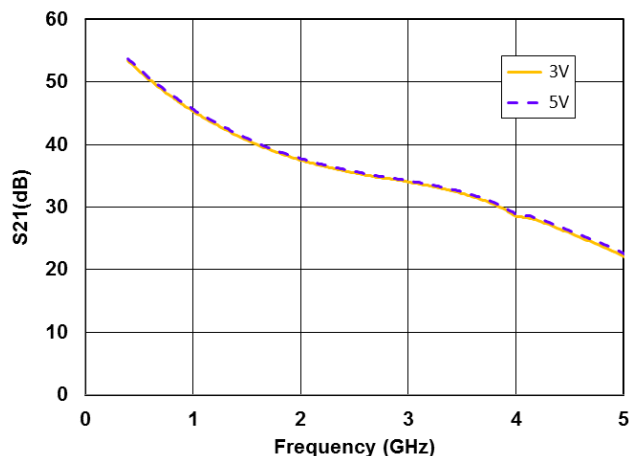


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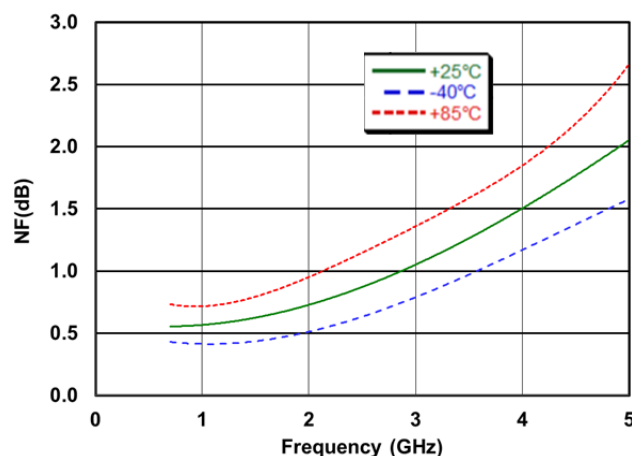
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Typical Performance Curves:  $T_A = +25^\circ\text{C}$ ,  $Z_0 = 50 \Omega$ ,  $V_{DD} = 3 \text{ V}$ , Switch State =  $\text{RF}_{\text{IN}} - \text{RF}_{\text{OUT}}$

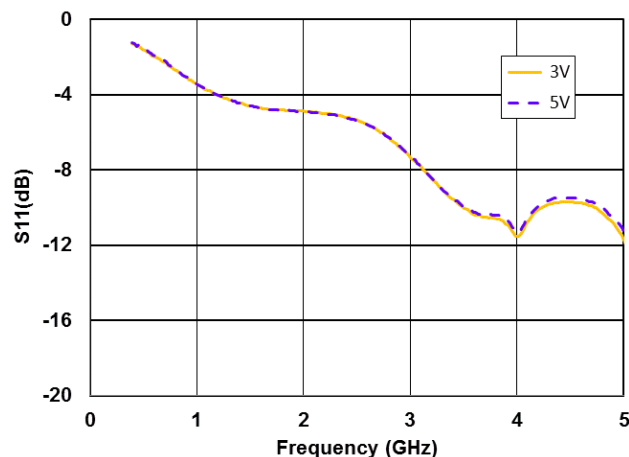
Gain vs. LNA1-2 Voltage



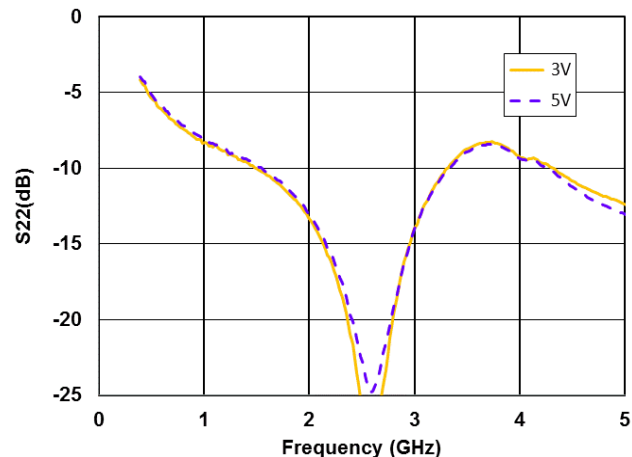
Noise Figure over Temperature,  $V_{DD} = 3 \text{ V}$



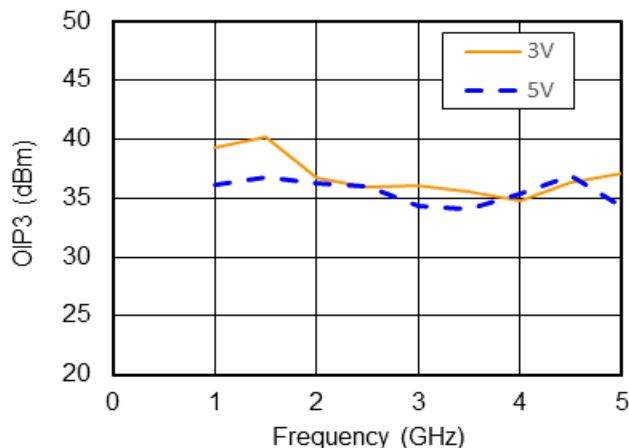
Input Return Loss vs. LNA1-2 Voltage



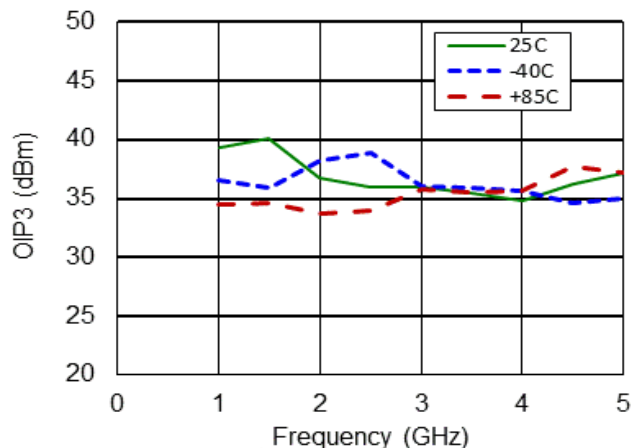
Output Return Loss vs. LNA1-2 Voltage



OIP3 vs. LNA1-2 Voltage

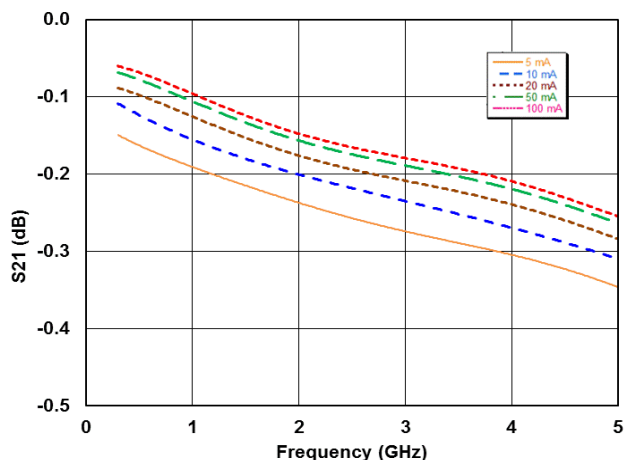


OIP3 over Temperature,  $V_{DD} = 3 \text{ V}$

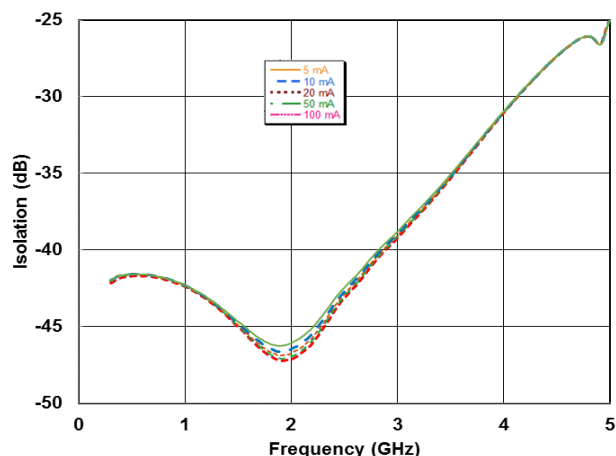


Typical Performance Curves:  $T_A = +25^\circ\text{C}$ ,  $Z_0 = 50 \Omega$ ,  $V_{DD} = 3 \text{ V}$ ,  $RF_{IN} - \text{LOAD}$

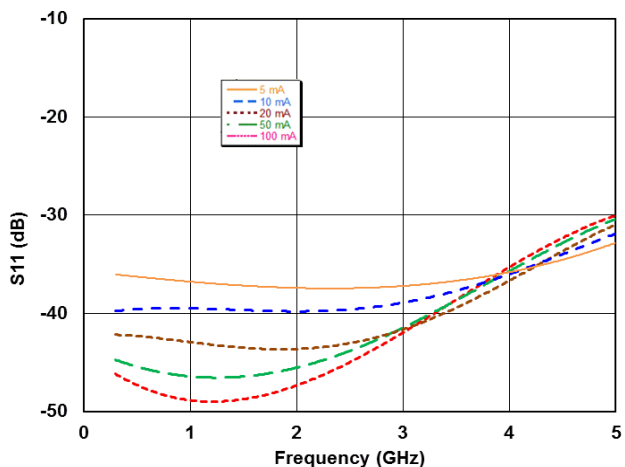
S21 vs. Switch Bias Current



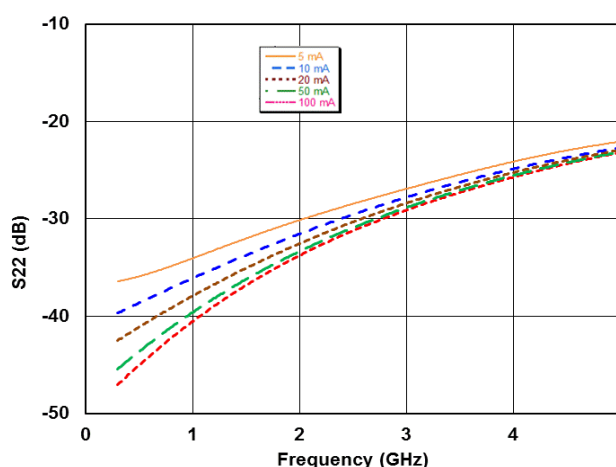
Isolation,  $RF_{IN}$  to  $LNA1_{IN}$  vs. Bias Current



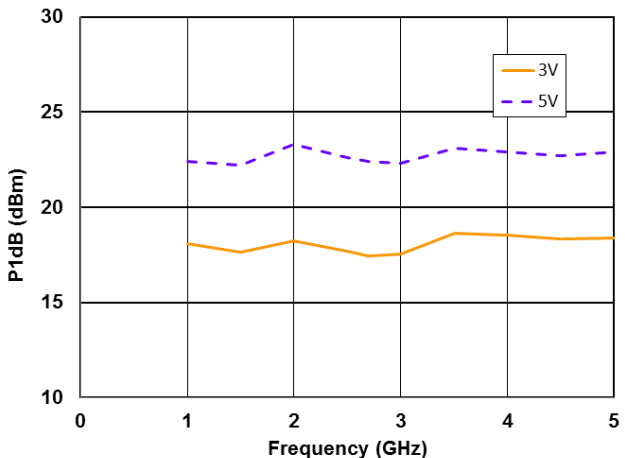
S11 vs. Switch Bias Current



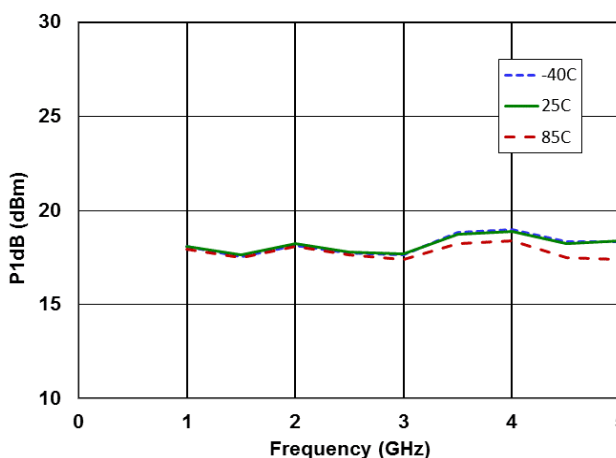
S22 vs. Switch Bias Current



P1dB vs.  $LNA1-2$  Voltage, State =  $RF_{IN} - RF_{OUT}$



P1dB vs. Temperature, State =  $RF_{IN} - RF_{OUT}$



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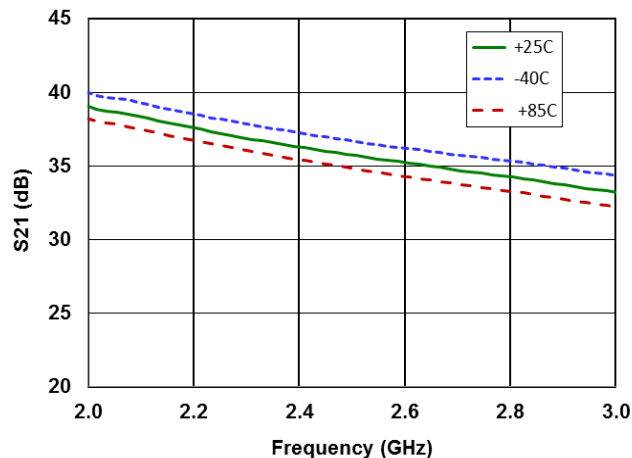
**Electrical Specifications:**  $T_A = +25^\circ\text{C}$ ,  $V_{DD1} = 3\text{ V}$ ,  $V_{BB1} = 3\text{ V}$ ,  $V_{DD2} = 3\text{ V}$ ,  $V_{BB2} = 3\text{ V}$ ,  
**Switch Bias = (see Bias Table),  $R5 = 133\ \Omega^{10}$ ,  $R7 = 100\ \Omega^{10}$ ; Tuned for 2 - 3 GHz band**

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	$RF_{IN} - RF_{OUT}$ , 2.7GHz	dB	31	34	—
Noise Figure	$RF_{IN} - RF_{OUT}$ , 2.7GHz	dB	—	1.1	1.5
Input Return Loss	$RF_{IN} - RF_{OUT}$ , 2.7GHz	dB	—	11	—
Output Return Loss	$RF_{IN} - RF_{OUT}$ , 2.7GHz	dB	—	18	—
LNA Bias Current	LNA1 Current: $I_{DD1} + I_{VB1}$ LNA2 Current: $I_{DD2} + I_{VB2}$	mA	—	75 65	—

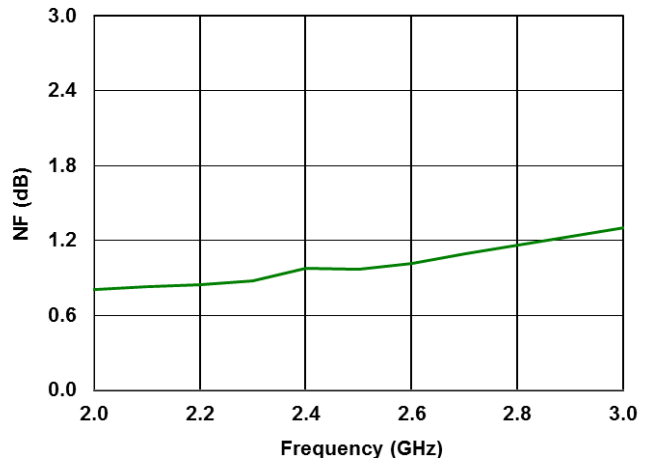
10. Refer to LNA Sample Board Schematic on page 9.

### Typical Performance Curves: 2 - 3 GHz tuned Sample Board, $RF_{IN} - RF_{OUT}$

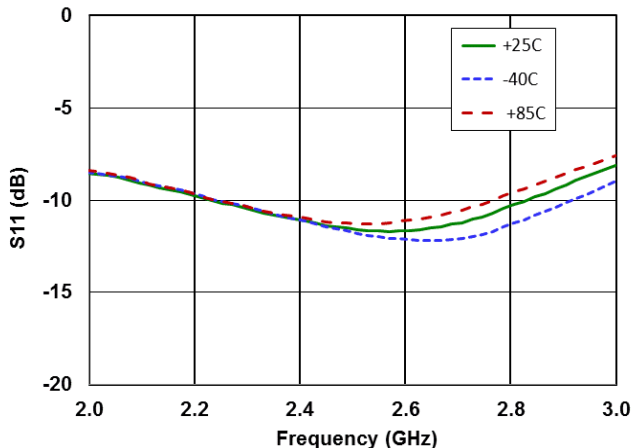
**Gain**



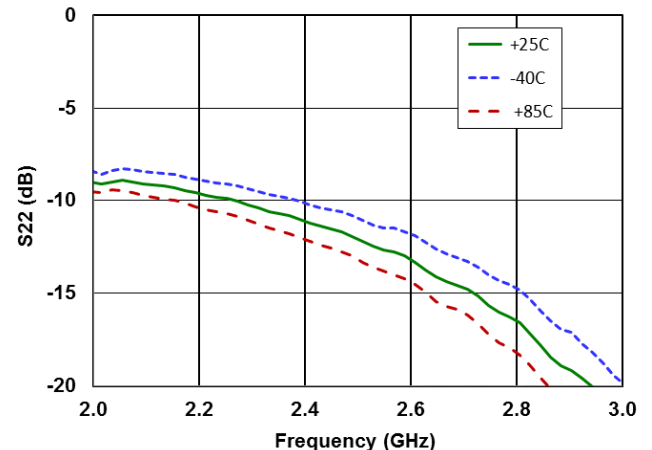
**Noise Figure**



**Input Return Loss**



**Output Return Loss**





# High Power Switch - LNA Module

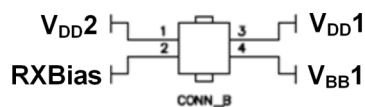
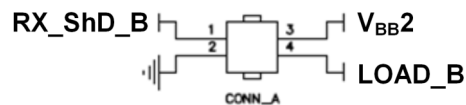
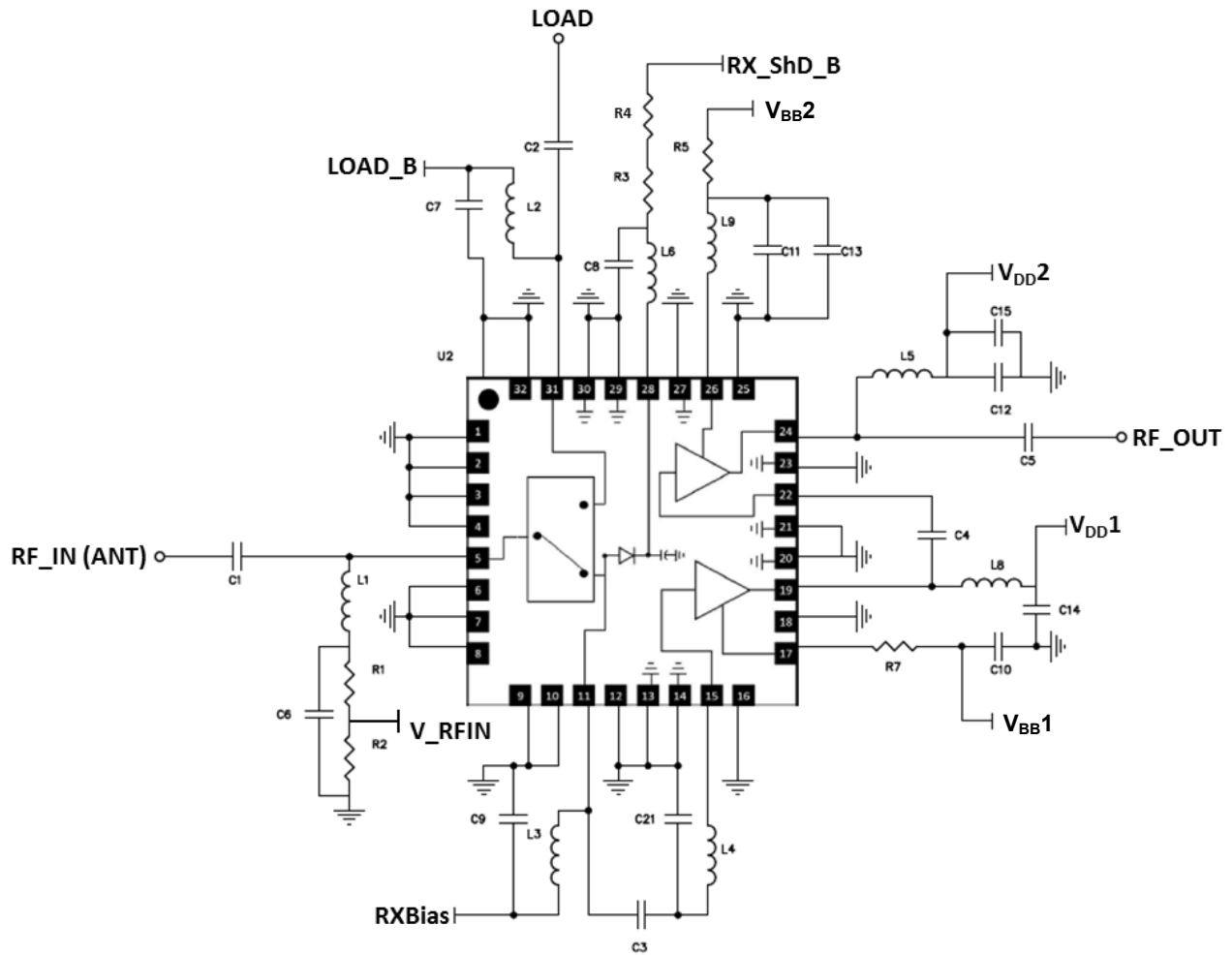
## 0.4 - 5.0 GHz



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### Schematic: MAIA-011004 Sample Board



# High Power Switch - LNA Module

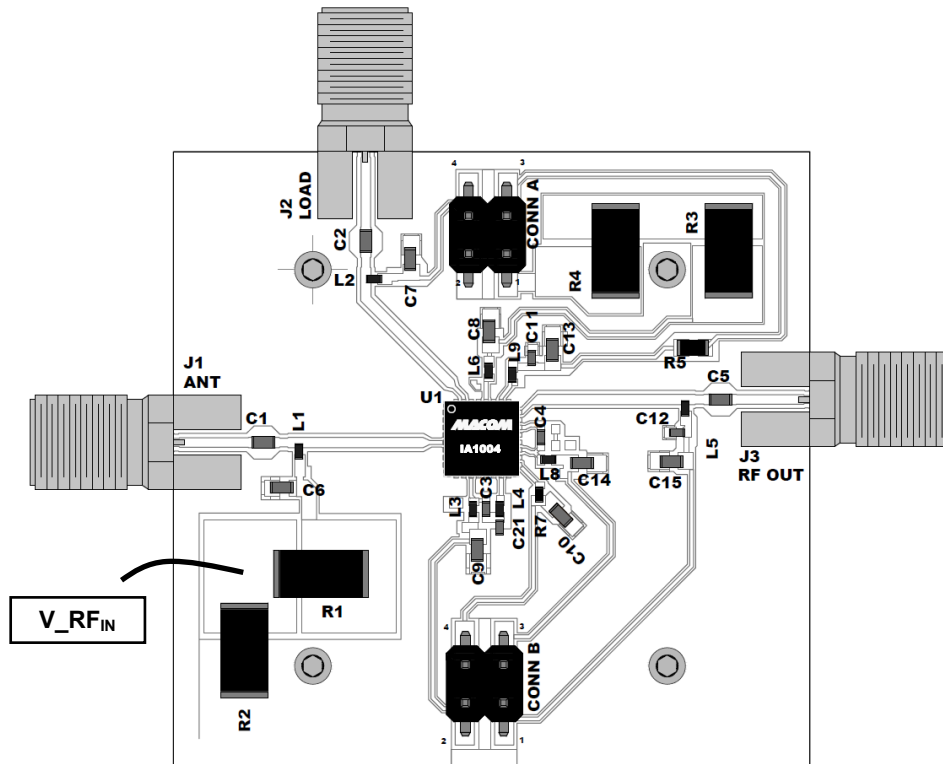
## 0.4 - 5.0 GHz



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### PCB Layout: MAIA-011004 Sample Board



### Sample Board Parts List\* for 2 - 3 GHz Tuned PCB

Part	Value	Description	MFR Part #
C1, C2, C5,	27 pF / 250 V	0603 SMT Capacitor	ATC600S270GT250T
C3	22 pF / 250 V	0402 SMT Capacitor	ATC600L220FT200T
C4	3.3 pF / 50 V	0402 SMT Capacitor	GRM1555C1H3R3BA01D
C6, C7, C8, C9, C10, C13, C14, C15	4.7 $\mu$ F / 35 V	0603 SMT Capacitor	—
C11	10 nF / 25V	0402 SMT Capacitor	—
C12	1 nF / 25V	0402 SMT Capacitor	—
C21	0.40 pF $\pm$ 0.1 pF	0402 SMT Capacitor	GJM1555C1HR40BB01
L1, L2, L3, L5, L6, L9	68 nH / 100 mA	0402 SMT Inductor	0402CS-68NXJLW
L4	2.7 nH	0402 SMT Inductor	0402CS-2N7XJLU
L8	2.0 nH	0402 SMT Inductor	0402CS-2N0XJLU
R1	45 $\Omega$ / 1.0 W	2512 SMT Resistor	—
R3, R4	270 $\Omega$ / 1.0 W	2512 SMT Resistor	—
R5 (R <sub>BIAS2</sub> )	133 $\Omega$	0805 SMT Resistor	—
R7 (R <sub>BIAS1</sub> )	100 $\Omega$	0402 SMT Resistor	—
J1 - J3	SMA END LAUNCH	RF CONNECTOR	142-0761-821
R2, C16, C18, C19, C20, C22		do not populate	

\* Aluminum heat sink mounted to backside of PCB is not shown

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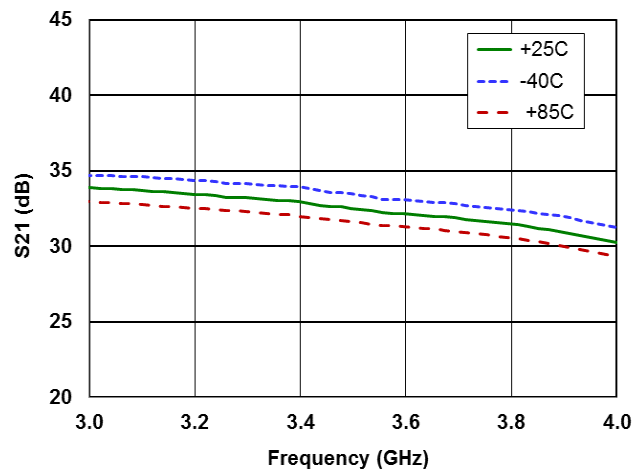
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**Electrical Specifications:**  $T_A = +25^\circ\text{C}$ ,  $V_{DD1} = 3\text{ V}$ ,  $V_{BB1} = 3\text{ V}$ ,  $V_{DD2} = 3\text{ V}$ ,  $V_{BB2} = 3\text{ V}$ ,  
**Switch Bias = (see Bias Table),  $R_5 = 133\ \Omega^{10}$ ,  $R_7 = 100\ \Omega^{10}$ ; Tuned for 3 - 4 GHz band**

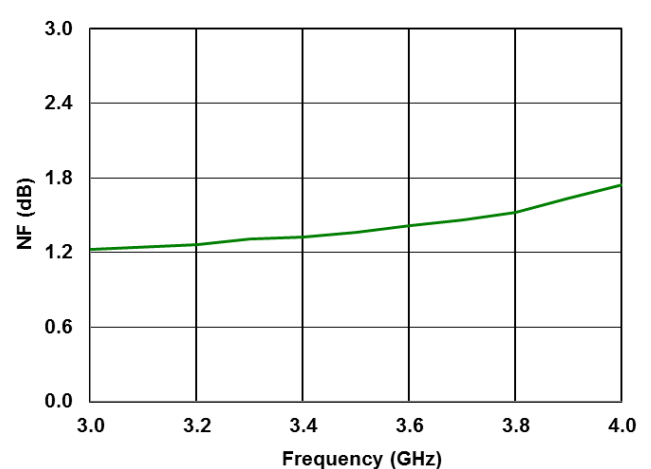
Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	$RF_{IN} - RF_{OUT}$ , 3.5 GHz	dB	—	32	—
Noise Figure	$RF_{IN} - RF_{OUT}$ , 3.5 GHz	dB	—	1.3	—
Input Return Loss	$RF_{IN} - RF_{OUT}$ , 3.5 GHz	dB	—	12	—
Output Return Loss	$RF_{IN} - RF_{OUT}$ , 3.5 GHz	dB	—	14	—
LNA Bias Current	LNA1 Current: $I_{DD1} + I_{VB1}$ LNA2 Current: $I_{DD2} + I_{VB2}$	mA	—	75 65	—

### Typical Performance Curves: 3 - 4 GHz tuned Sample Board, $RF_{IN} - RF_{OUT}$

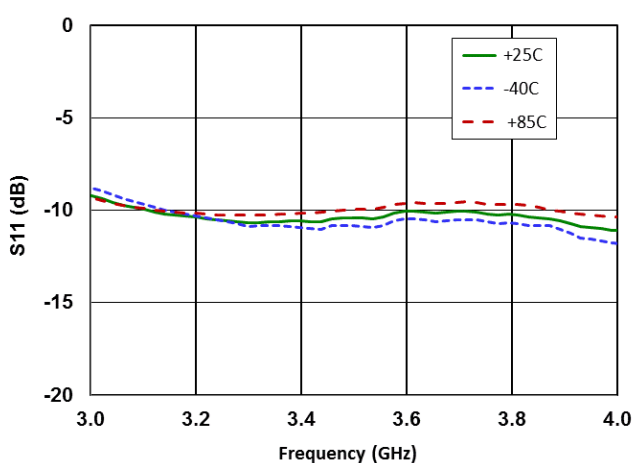
**Gain**



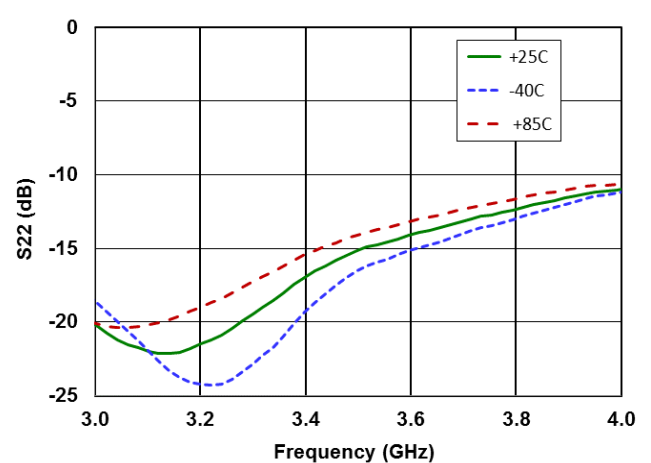
**Noise Figure**



**Input Return Loss**



**Output Return Loss**



# High Power Switch - LNA Module

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### Sample Board Parts List\* for 3 - 4 GHz Tuned PCB

Part	Value	Description	MFR Part #
C1, C2, C5	27 pF / 250 V	0603 SMT Capacitor	ATC600S270GT250T
C3	22 pF / 250 V	0402 SMT Capacitor	ATC600L220FT200T
C4, C12	1000 pF / 25 V	0402 SMT Capacitor	—
C6, C7, C8, C9, C10, C13, C14, C15	4.7 $\mu$ F / 35 V	0603 SMT Capacitor	—
C11	10 nF / 25V	0402 SMT Capacitor	—
C21	0.50 pF $\pm$ 0.1 pF	0402 SMT Capacitor	GJM1555C1HR50BB01
L1, L2, L3, L5 ,L6, L9	68 nH / 100 mA	0402 SMT Inductor	0402CS-68NXJLW
L4	1.2 nH	0402 SMT Inductor	0402CS-1N2XJLU
L8	2.0 nH	0402 SMT Inductor	0402CS-2N0XJLU
R1	45 $\Omega$ / 1.0 W	2512 SMT Resistor	—
R3, R4	270 $\Omega$ / 1.0 W	2512 SMT Resistor	—
R5 (R <sub>BIAS2</sub> )	133 $\Omega$	0805 SMT Resistor	—
R7 (R <sub>BIAS1</sub> )	100 $\Omega$	0402 SMT Resistor	—
J1 - J3	SMA END LAUNCH	RF CONNECTOR	142-0761-821
R2, C16, C18, C19, C20, C22	do not populate		
* Aluminum heat sink mounted to backside of PCB is not shown			

# High Power Switch - LNA Module

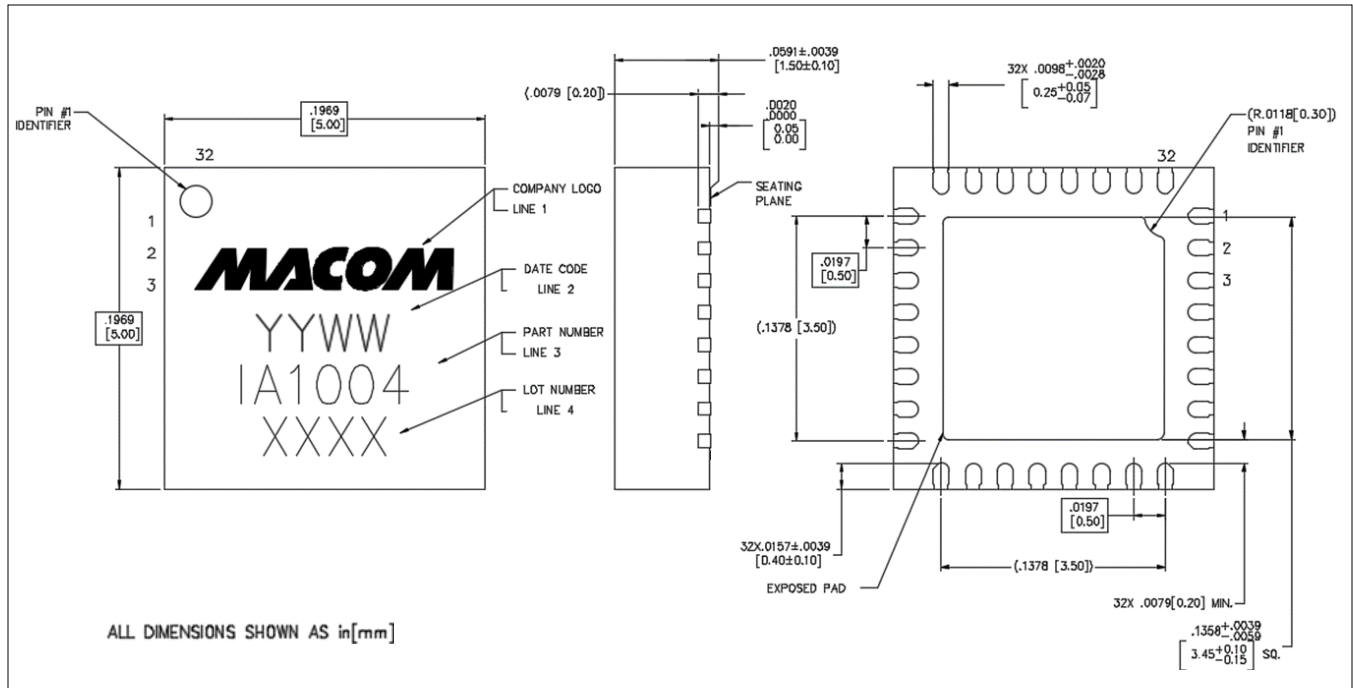
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MAIA-011004

Rev. V3

### Lead-Free 5 mm 32-Lead HQFN<sup>†</sup>



<sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations.  
 Meets JEDEC moisture sensitivity level 1 requirements.  
 Plating is NiPdAuAg.

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