SN54LV4053A, SN74LV4053A
TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

- **2-V to 5.5-V V_{CC} Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **High On-Off Output-Voltage Ratio**
- **Low Crosstalk Between Switches**
- **Individual Switch Controls**
- **Extremely Low Input Current**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV4053A . . . J OR W PACKAGE
SN74LV4053A . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)

2Y1	1	16	V_{CC}
2Y0	2	15	2-COM
3Y1	3	14	1-COM
3-COM	4	13	1Y1
3Y0	5	12	1Y0
INH	6	11	A
GND	7	10	B
GND	8	9	C
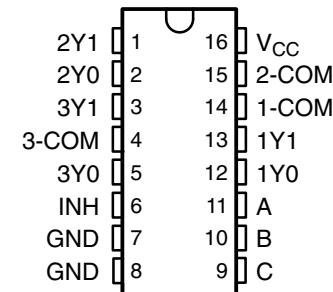
SN74LV4053A . . . RGY PACKAGE
(TOP VIEW)

2Y0	2	15	2-COM
3Y1	3	14	1-COM
3-COM	4	13	1Y1
3Y0	5	12	1Y0
INH	6	11	A
GND	7	10	B

Top pins: 2Y1 (1), V_{CC} (16). Bottom pins: GND (8), C (9).
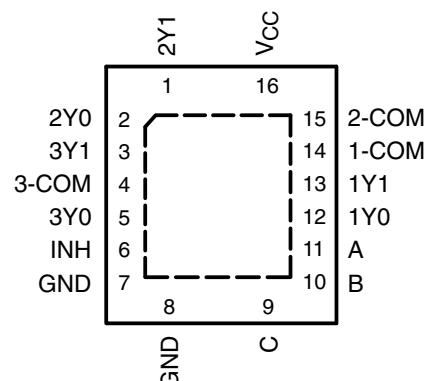
description/ordering information

These triple 2-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV4053A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube of 25	SN74LV4053AN	SN74LV4053AN
	QFN – RGY	Reel of 1000	SN74LV4053ARGYR	LW053A
	SOIC – D	Tube of 40	SN74LV4053AD	LV4053A
		Reel of 2500	SN74LV4053ADR	
	SOP – NS	Reel of 2000	SN74LV4053ANSR	74LV4053A
	SSOP – DB	Reel of 2000	SN74LV4053ADBR	LW053A
	TSSOP – PW	Tube of 90	SN74LV4053APW	LW053A
		Reel of 2000	SN74LV4053APWR	
		Reel of 250	SN74LV4053APWT	
	TVSOP – DGV	Reel of 2000	SN74LV4053ADGVR	LW053A
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV4053AJ	SNJ54LV4053AJ
	CFP – W	Tube of 150	SNJ54LV4053AW	SNJ54LV4053AW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

SN54LV4053A, SN74LV4053A
TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

FUNCTION TABLE

INPUTS				ON CHANNELS
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None

logic diagram (positive logic)
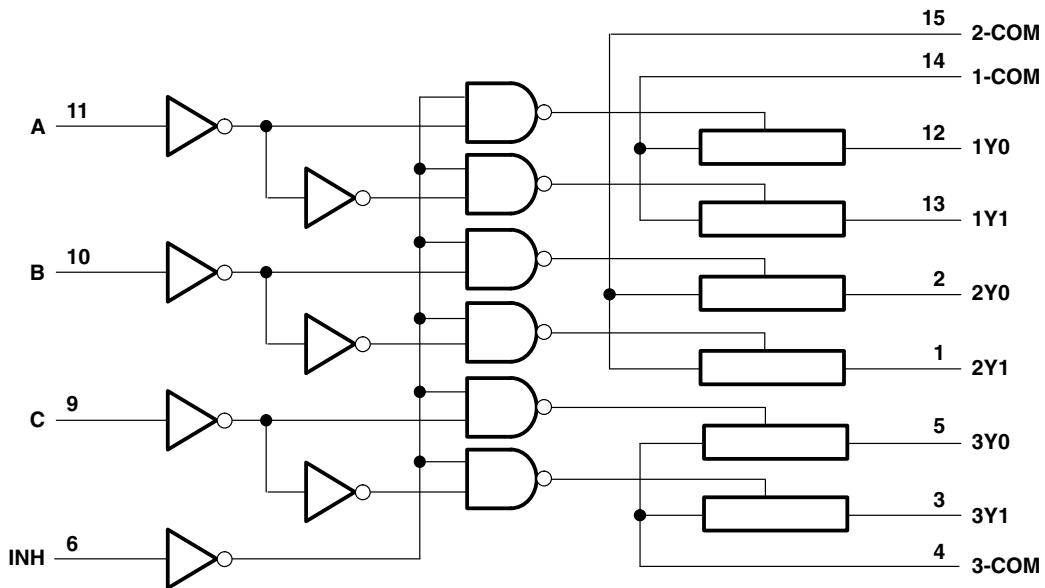
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . –20 mA
I/O diode current, I_{IOK} (V_{IO} < 0) . . . . –50 mA
Switch through current, I_T (V_{IO} = 0 to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . 73°C/W
(see Note 3): DB package . . . . 82°C/W
(see Note 3): DGV package . . . . 120°C/W
(see Note 3): NS package . . . . 64°C/W
(see Note 3): PW package . . . . 108°C/W
(see Note 4): RGY package . . . . 39°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV4053A		SN74LV4053A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2‡	5.5	2‡	5.5	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Control input voltage		0	5.5	0	5.5	V
V_{IO}	Input/output voltage		0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

‡ With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54LV4053A		SN74LV4053A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r_{on}	On-state switch resistance	$I_T = 2$ mA, $V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 1)	2.3 V		41	180		225		225	Ω
			3 V		30	150		190		190	
			4.5 V		23	75		100		100	
$r_{on(p)}$	Peak on-state resistance	$I_T = 2$ mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$	2.3 V		139	500		600		600	Ω
			3 V		63	180		225		225	
			4.5 V		35	100		125		125	
Δr_{on}	Difference in on-state resistance between switches	$I_T = 2$ mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$	2.3 V		2	30		40		40	Ω
			3 V		1.6	20		30		30	
			4.5 V		1.3	15		20		20	
I_I	Control input current	$V_I = 5.5$ V or GND	0 to 5.5 V			±0.1		±1		±1	µA
$I_{S(off)}$	Off-state switch leakage current	$V_I = V_{CC}$ and $V_O = $ GND, or $V_I = $ GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 2)	5.5 V			±0.1		±1		±1	µA
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IH}$ (see Figure 3)	5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	5.5 V					20		20	µA
C_{IC}	Control input capacitance				2						pF
C_{IS}	Common terminal capacitance				8.2						pF
C_{OS}	Switch terminal capacitance				5.6						pF
C_F	Feedthrough capacitance				0.5						pF

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5$ V $\pm$ 0.2 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25°C$			SN54LV4053A		SN74LV4053A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 15$ pF (see Figure 4)		2.5	10		16		16	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 15$ pF (see Figure 5)		7.6	18		23		23	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 15$ pF (see Figure 5)		7.7	18		23		23	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50$ pF (see Figure 4)		4.4	12		18		18	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50$ pF (see Figure 5)		8.8	28		35		35	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50$ pF (see Figure 5)		11.7	28		35		35	ns

![Texas Instruments logo]

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF (see Figure 4)		1.6	6		10		10	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 5)		5.3	12		15		15	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 5)		6.1	12		15		15	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF (see Figure 4)		2.9	9		12		12	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 5)		6.1	20		25		25	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 5)		8.9	20		25		25	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			SN54LV4053A		SN74LV4053A		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 15 pF (see Figure 4)		0.9	4		7		7	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 5)		3.8	8		10		10	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 15 pF (see Figure 5)		4.6	8		10		10	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	C_L = 50 pF (see Figure 4)		1.8	6		8		8	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 5)		4.3	14		18		18	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	C_L = 50 pF (see Figure 5)		6.3	14		18		18	ns

TEXAS INSTRUMENTS

analog switch characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	T_A = 25°C TYP	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 6 and Figure 6)		2.3 V	30	MHz
					3 V	35	
					4.5 V	50	
Crosstalk (between any switches)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Note 7 and Figure 7)		2.3 V	−45	dB
					3 V	−45	
					4.5 V	−45	
Crosstalk (control input to signal output)	INH	COM or Yn	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)		2.3 V	20	mV
					3 V	35	
					4.5 V	65	
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (see Note 7 and Figure 9)		2.3 V	−45	dB
					3 V	−45	
					4.5 V	−45	
Sine-wave distortion	COM or Yn	Yn or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	V_I = 2 V_{p-p}	2.3 V	0.1	%
				V_I = 2.5 V_{p-p}	3 V	0.1	
				V_I = 4 V_{p-p}	4.5 V	0.1	

NOTES: 6. Adjust f_{in} voltage to obtain 0-dBm output. Increase f_{in} frequency until dB meter reads −3 dB.
7. Adjust f_{in} voltage to obtain 0-dBm input.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	5.3	pF

PARAMETER MEASUREMENT INFORMATION

$$r_{on} = \frac{V_I - V_O}{2 \times 10^{-3}} \; \Omega$$
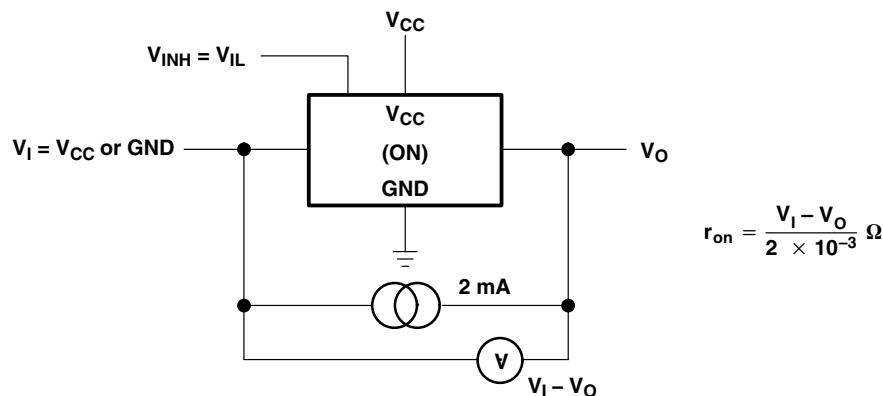
Figure 1. On-State Resistance Test Circuit

PARAMETER MEASUREMENT INFORMATION

V_{CC}

$V_{INH} = V_{IH}$

V_I — Ⓐ

V_{CC}

(OFF)

GND

V_O
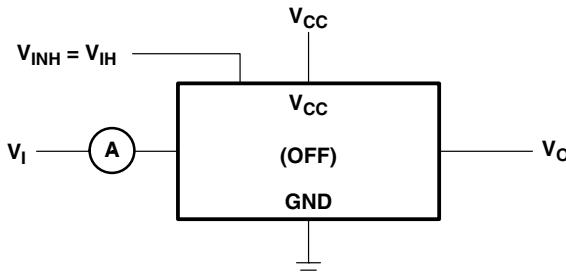
Condition 1: $V_I = 0$, $V_O = V_{CC}$
Condition 2: $V_I = V_{CC}$, $V_O = 0$

Figure 2. Off-State Switch Leakage-Current Test Circuit

V_{CC}

$V_{INH} = V_{IL}$

V_I — Ⓐ

V_{CC}

(ON)

GND

Open

$V_I = V_{CC}$ or GND
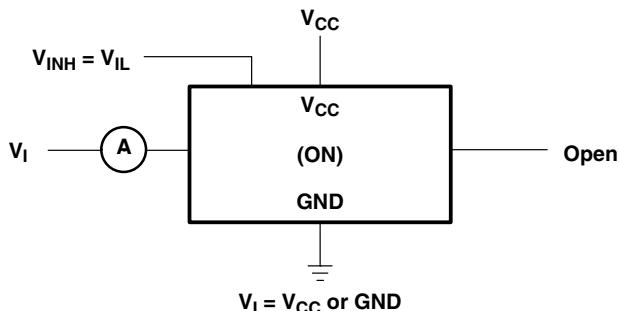
Figure 3. On-State Switch Leakage-Current Test Circuit

V_{CC}

$V_{INH} = V_{IL}$

Input

V_{CC}

(ON)

GND

Output

50 Ω

C_L
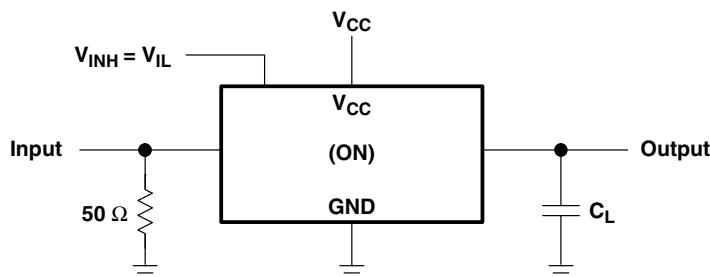
Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION

TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND
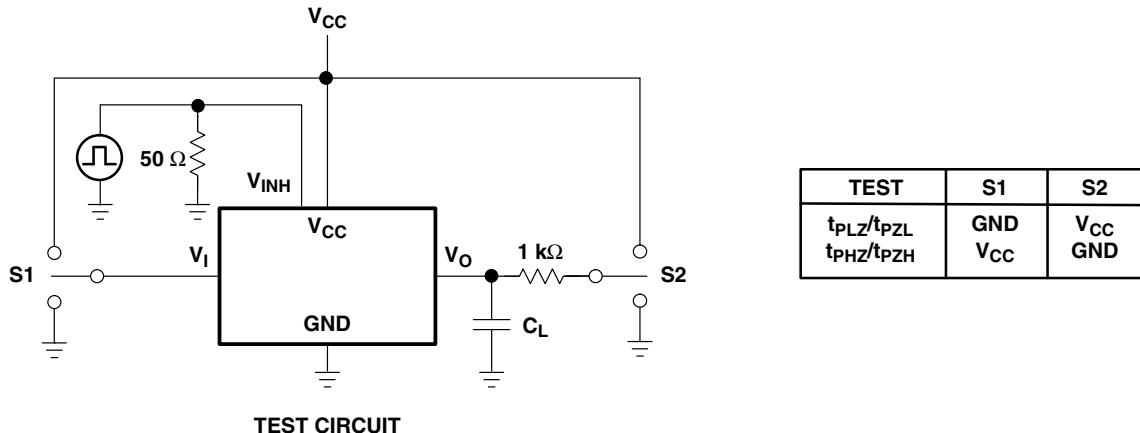
TEST CIRCUIT
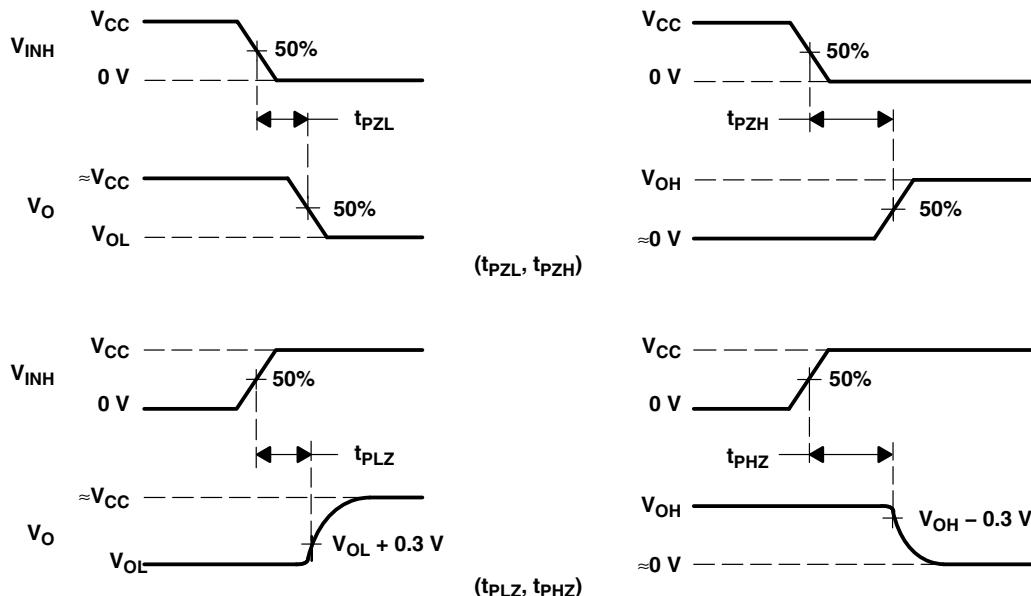

VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output
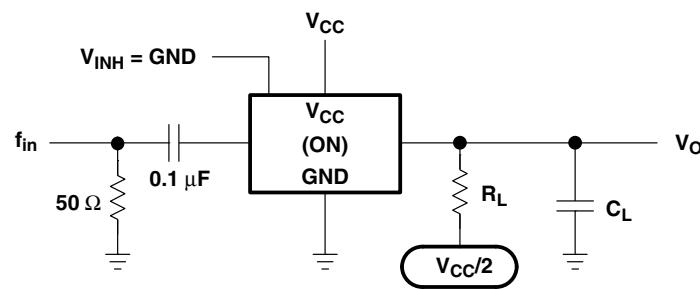
NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

## PARAMETER MEASUREMENT INFORMATION
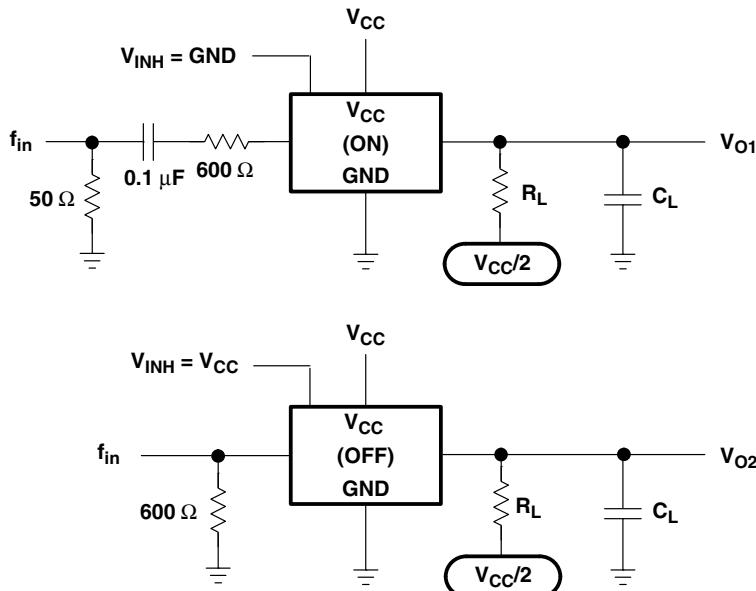
Figure 7. Crosstalk Between Any Two Switches
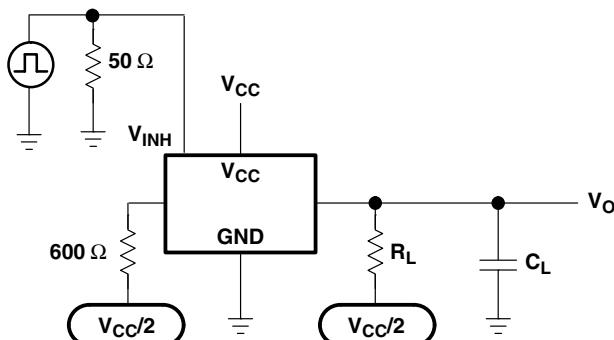
**Figure 8. Crosstalk Between Control Input and Switch Output**
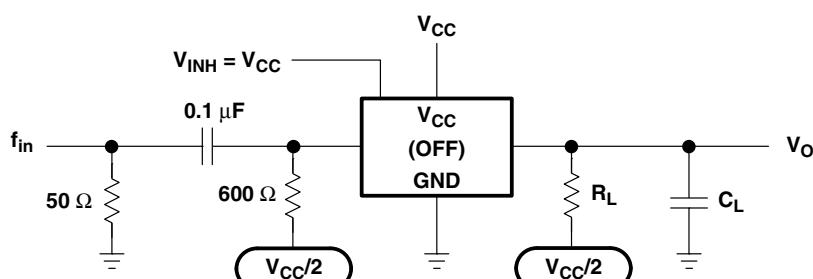
Figure 9. Feedthrough Attenuation (Switch Off)

## PARAMETER MEASUREMENT INFORMATION
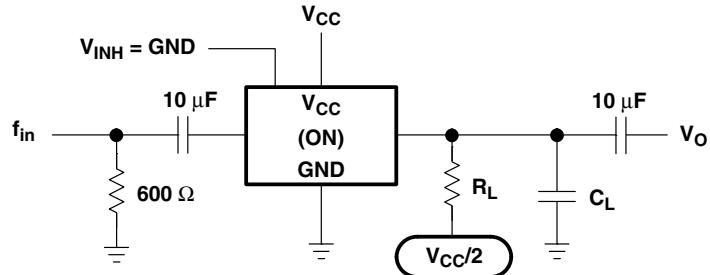
Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4053AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4053A	Samples
SN74LV4053ADBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053ADE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4053A	Samples
SN74LV4053ADGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053ADGVRG4	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LV4053A	Samples
SN74LV4053ADRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4053A	Samples
SN74LV4053AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4053AN	Samples
SN74LV4053ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4053AN	Samples
SN74LV4053ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4053A	Samples
SN74LV4053APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053APWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053APWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053APWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW053A	Samples
SN74LV4053ARGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW053A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4053A :

- Automotive: SN74LV4053A-Q1

- Enhanced Product: SN74LV4053A-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
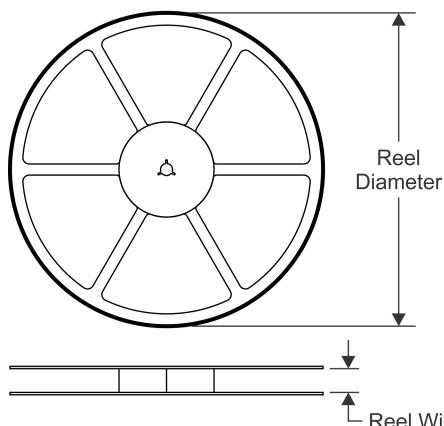
TAPE DIMENSIONS
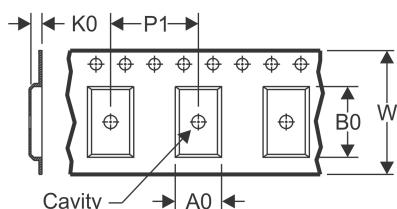
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
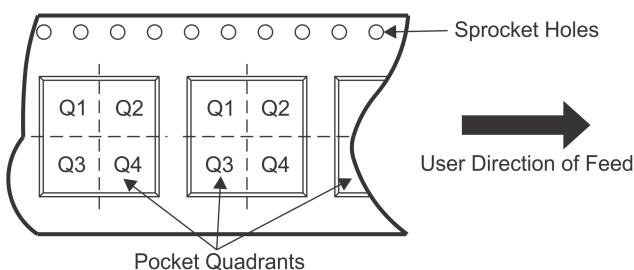
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4053ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4053ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4053ADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4053ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4053ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4053ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4053APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4053APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4053APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4053APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4053ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
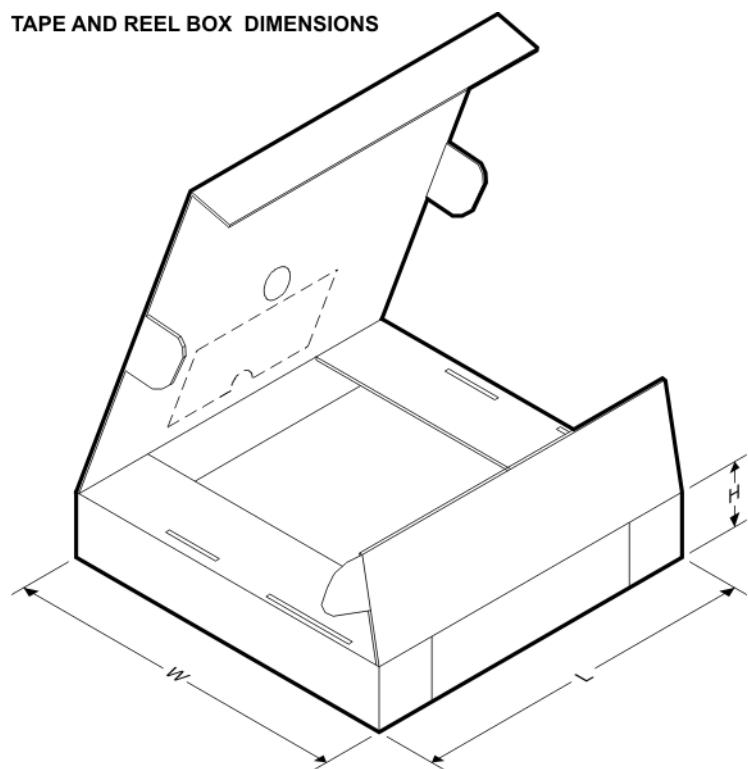
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4053ADBR	SSOP	DB	16	2000	853.0	449.0	35.0
SN74LV4053ADGVR	TVSOP	DGV	16	2000	853.0	449.0	35.0
SN74LV4053ADR	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV4053ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4053ADRG4	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4053ANSR	SO	NS	16	2000	853.0	449.0	35.0
SN74LV4053APWR	TSSOP	PW	16	2000	853.0	449.0	35.0
SN74LV4053APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV4053APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4053APWT	TSSOP	PW	16	250	853.0	449.0	35.0
SN74LV4053ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
△C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)
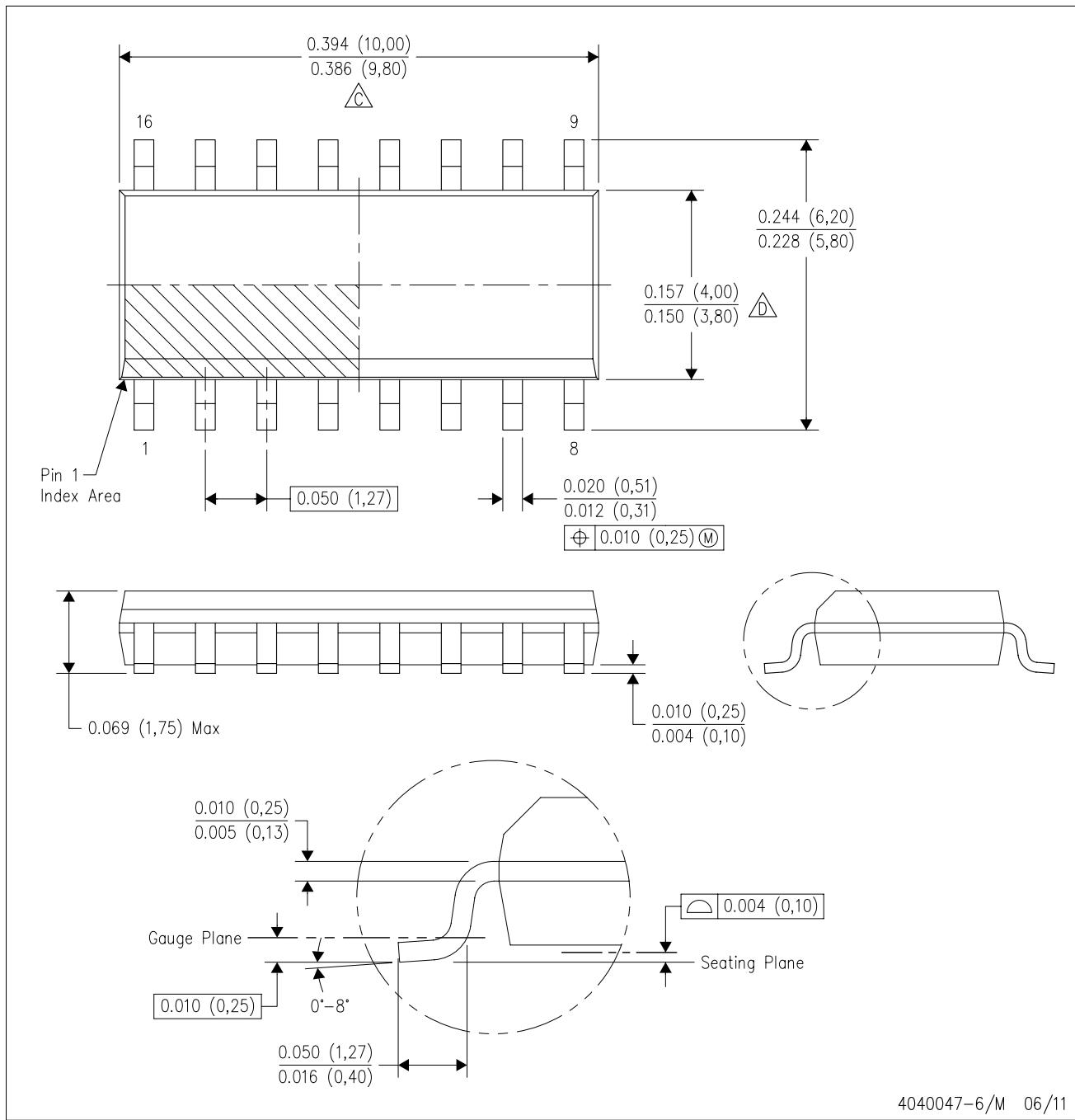
4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
      △C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
      △D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

TEXAS
INSTRUMENTS
www.ti.com

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

16x1,50

14x1,27

5,40

5.40
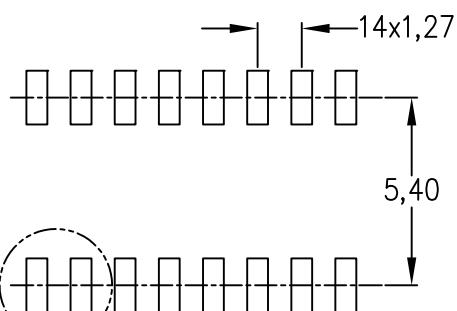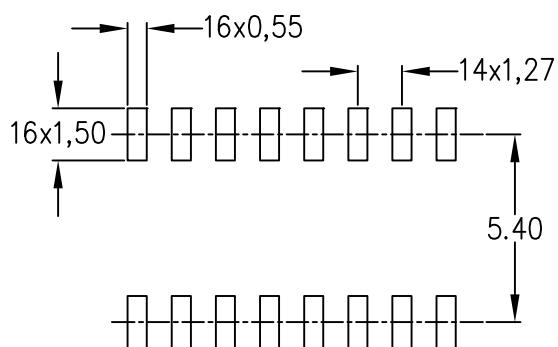
Example
Non Soldermask Defined Pad
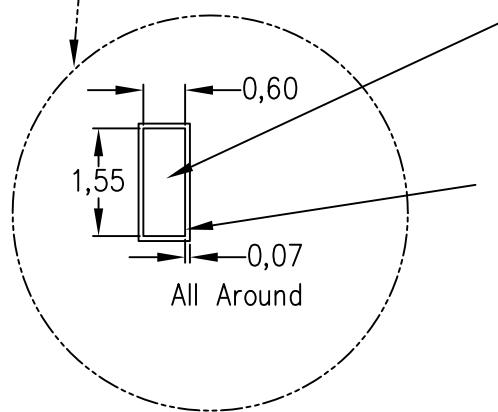
Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

SEATING PLANE

6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

C

0.1 C

1

2X

4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3
NOTE 4

16X 0.30
0.19

1.2 MAX

⊕ 0.1ⓜ C A B

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0° -8°

0.75
0.50

DETAIL A
TYPICAL

4220204/A   02/2017
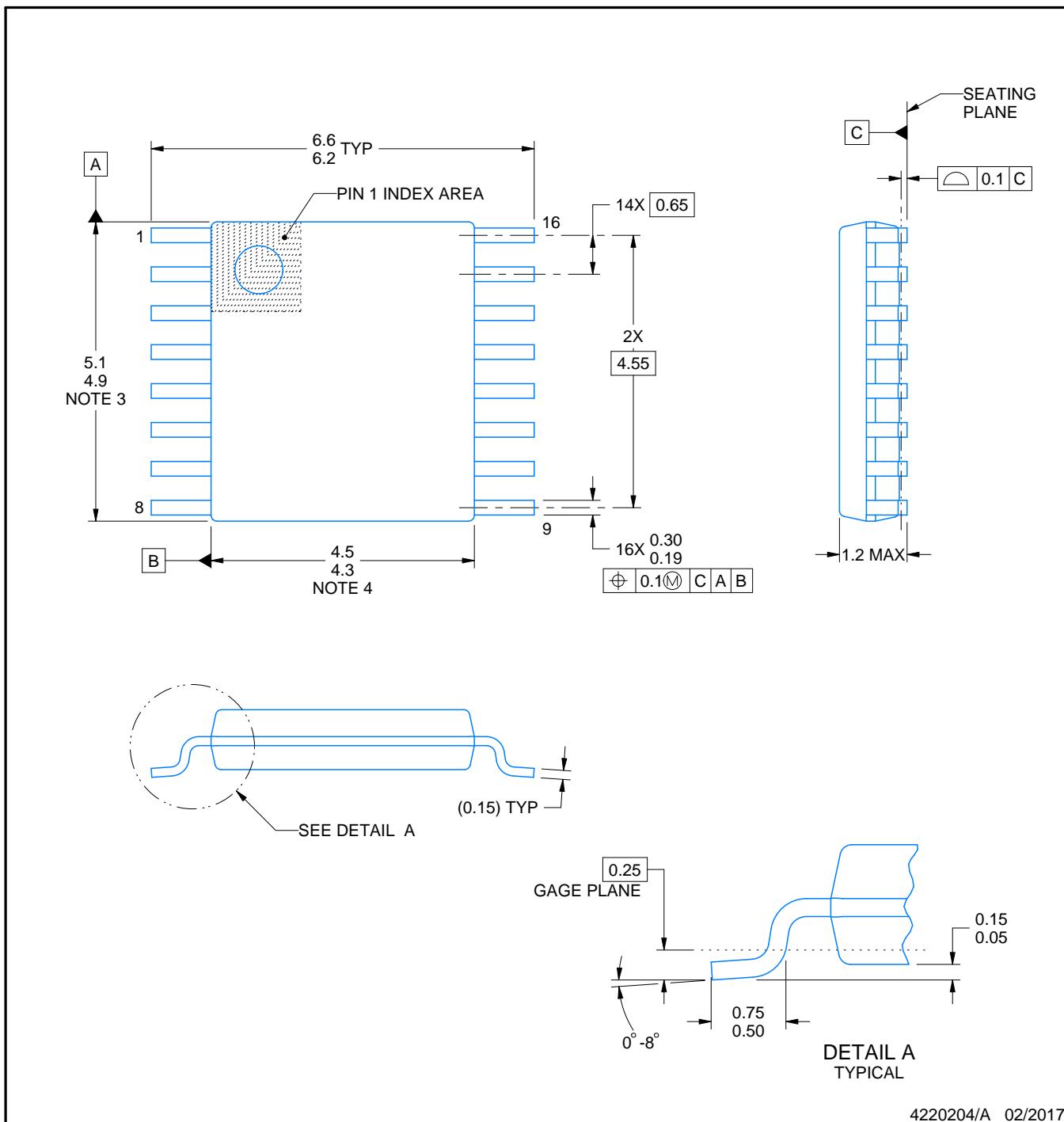
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)
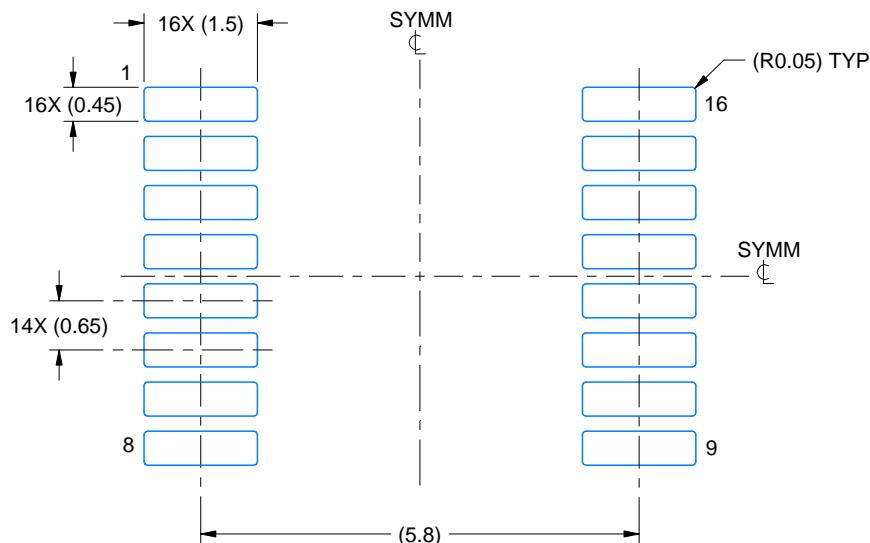
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
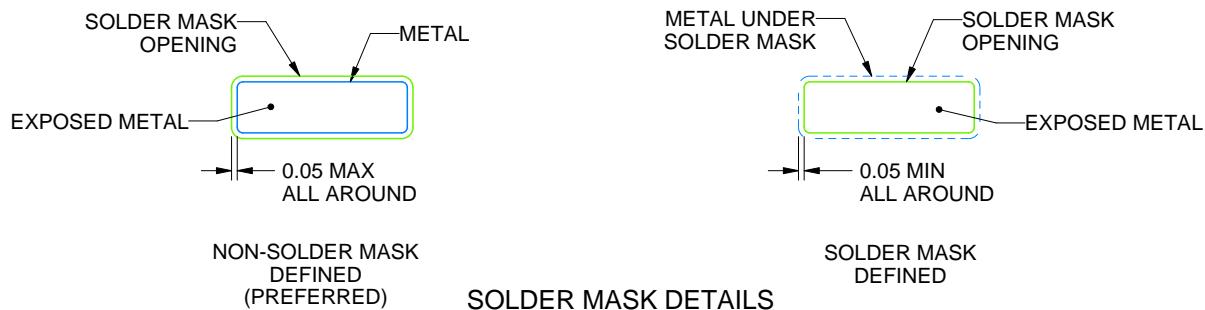
4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)
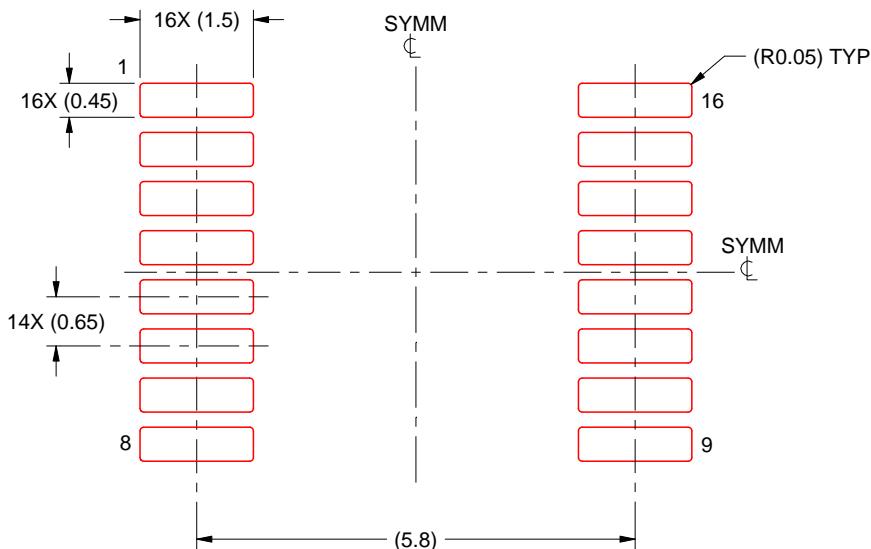
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NS (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE
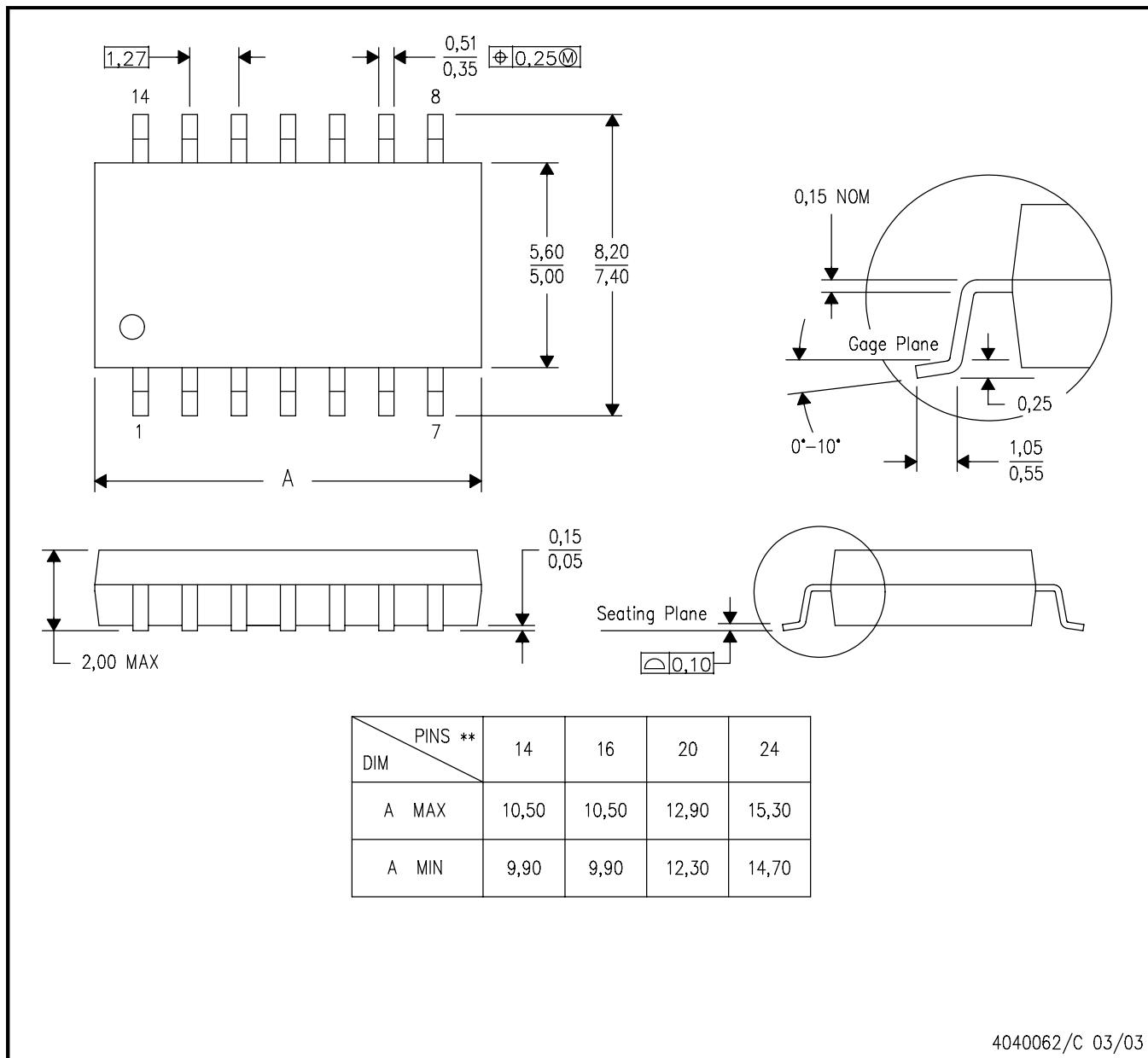
14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
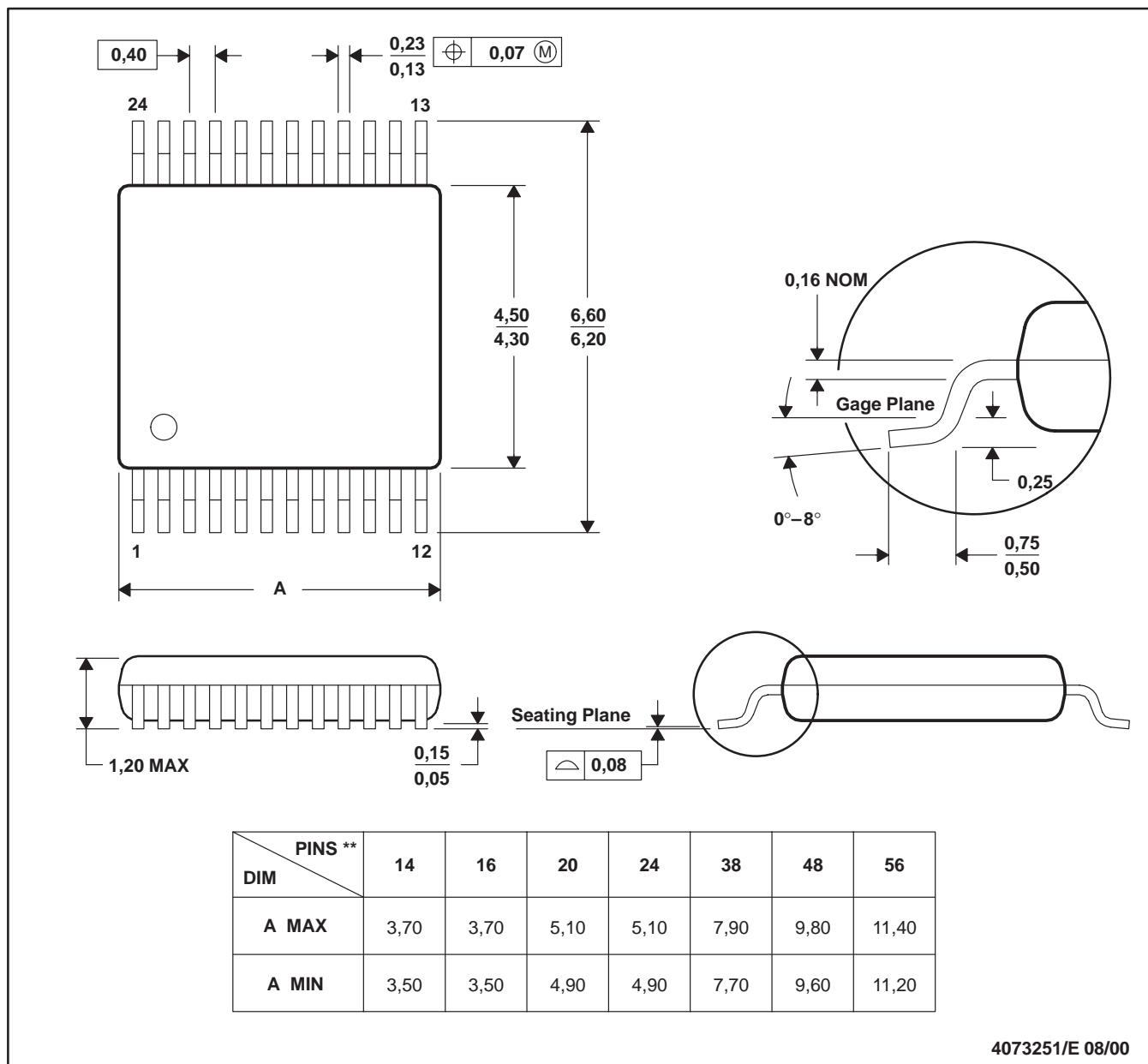
0,40

0,23
0,13 ⊕ | 0,07 Ⓜ

24　　　　　　　　　　13

4,50
4,30

6,60
6,20

0,16 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1　　　　　　　　　　12

A

1,20 MAX

0,15
0,05

Seating Plane

⌒ | 0,08

DIM ╲ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
　　　　B. This drawing is subject to change without notice.
　　　　C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
　　　　D. Falls within JEDEC: 24/48 Pins – MO-153
　　　　　　　　　　　　　　　14/16/20/56 Pins – MO-194

N (R−PDIP−T**)
16 PINS SHOWN

## PLASTIC DUAL−IN−LINE PACKAGE
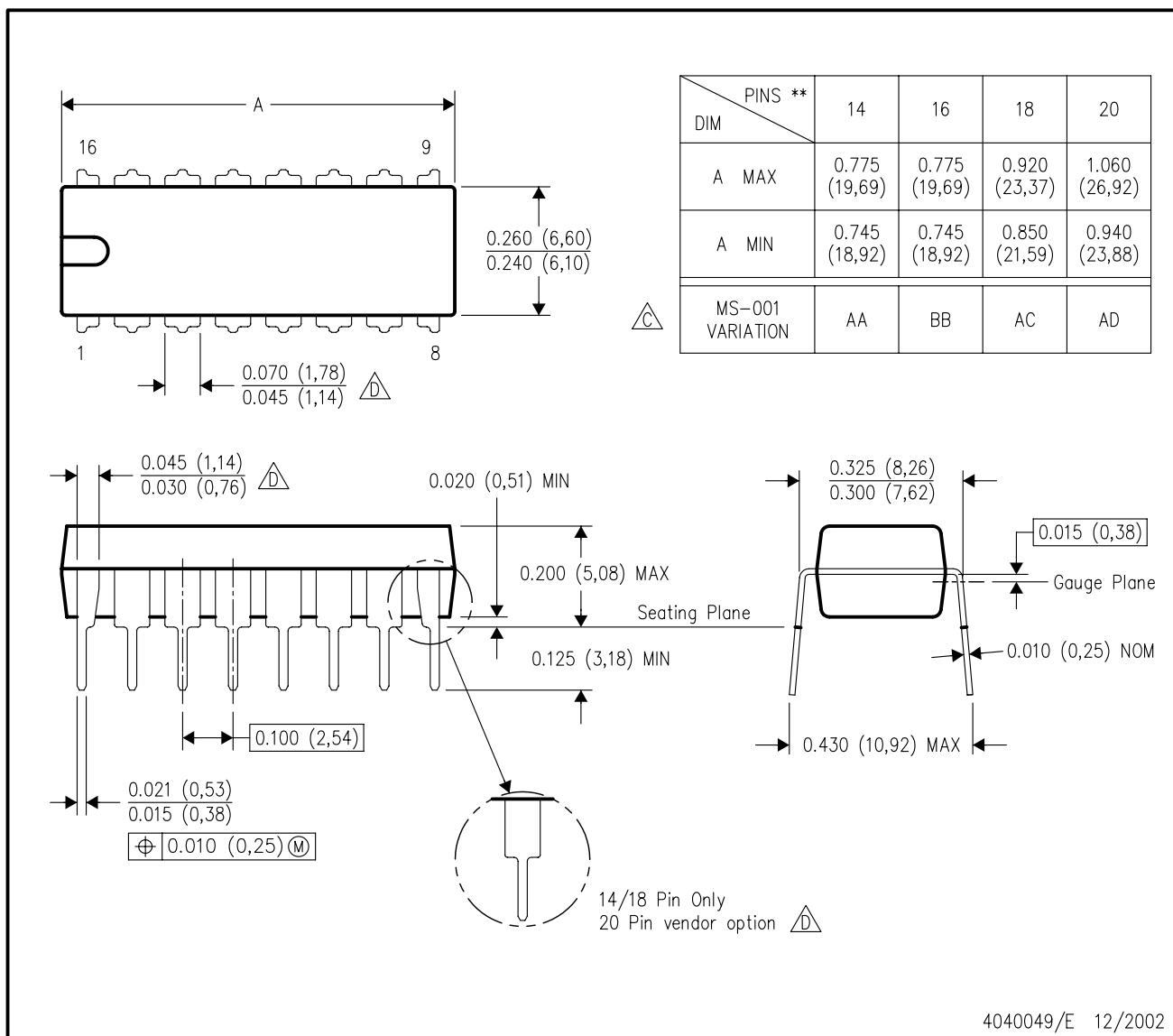
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) /D\

0.045 (1,14)
0.030 (0,76) /D\

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

/C\

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
    B. This drawing is subject to change without notice.
    /C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
    /D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS
www.ti.com

RGY (R–PVQFN–N16)   PLASTIC QUAD FLATPACK NO–LEAD

$\frac{4,15}{3,85}$ [A]

[B]

15   10

16   9

$\frac{3,65}{3,35}$

1   8

2   7

Pin 1 Index Area
Top and Bottom
[F]

$\frac{1,00}{0,80}$

0,20 Nominal
Lead Frame

Seating Plane

| ⌒ | 0,08 | C |

$\frac{0,05}{0,00}$
Seating Height

[C]

2,50

0,50

16X $\frac{0,50}{0,30}$

2   7

1   8

THERMAL PAD

1,50

SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

9

16

15   10

16X $\frac{0,30}{0,18}$

| ⌖ | 0,10 Ⓜ | C | A | B |
| | 0,05 Ⓜ | C | | |
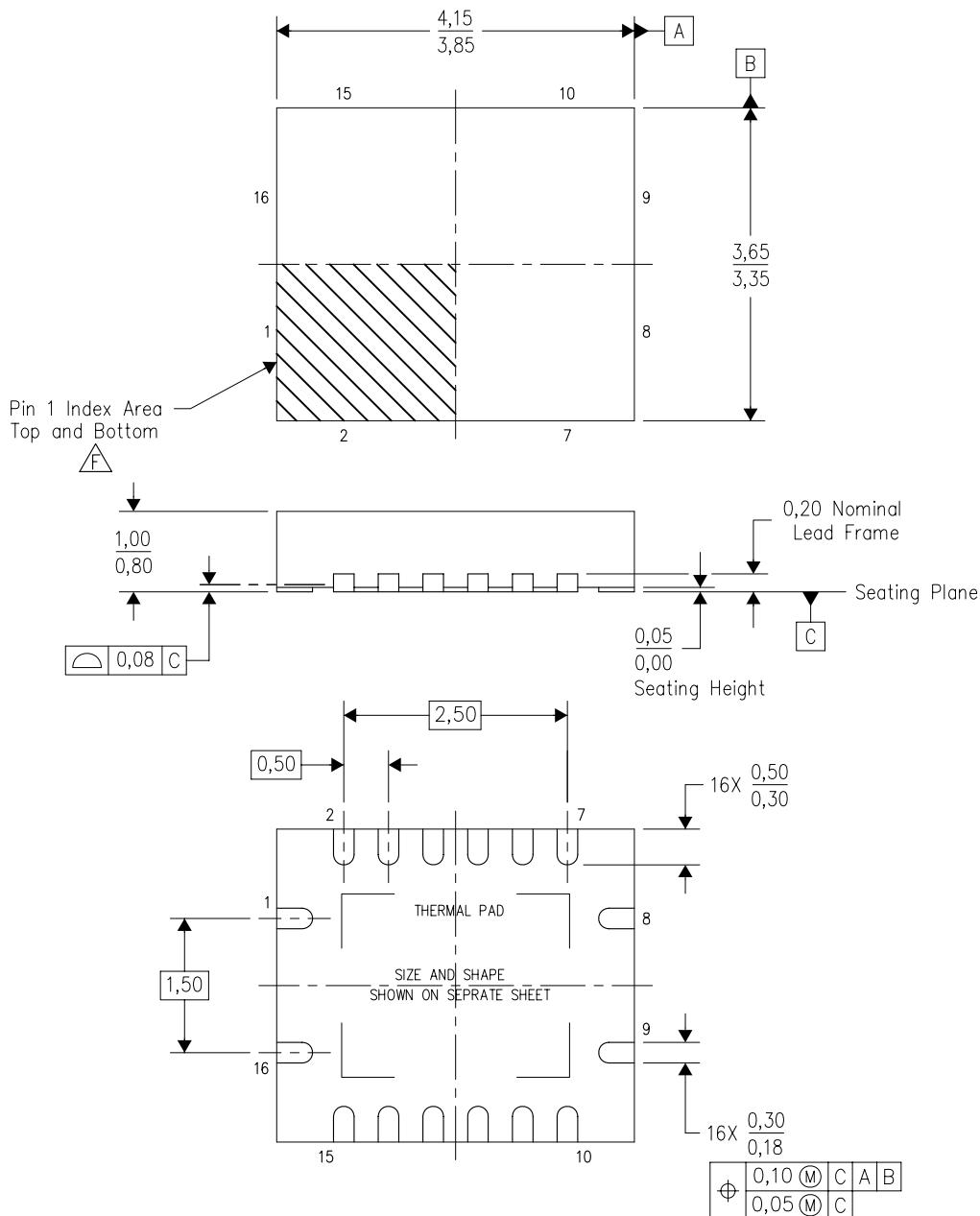
Bottom View

4203539–3/I   06/2011

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M–1994.
          B.   This drawing is subject to change without notice.
          C.   QFN (Quad Flatpack No–Lead) package configuration.
          D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
          E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
    [F]   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
          The Pin 1 identifiers are either a molded, marked, or metal feature.
          G.   Package complies to JEDEC MO–241 variation BA.

RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
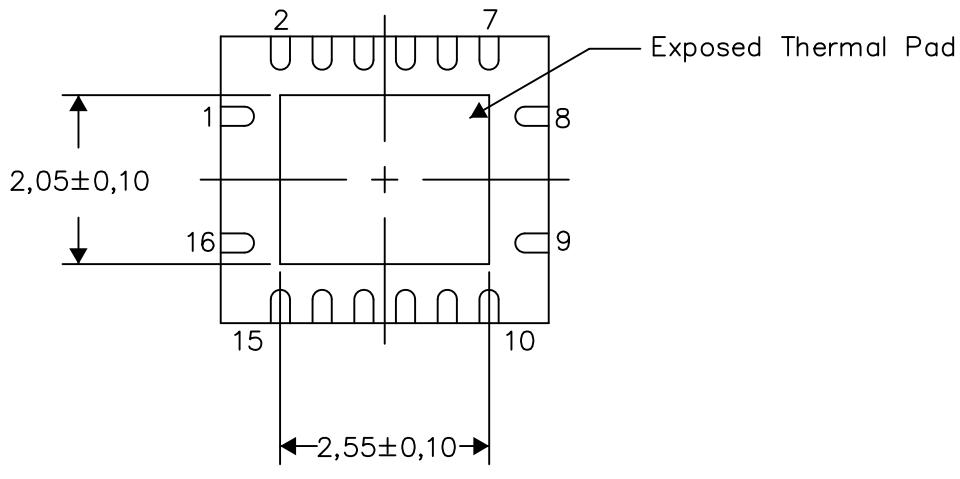
Bottom View

Exposed Thermal Pad Dimensions

4206353−3/P   03/14

NOTE: All linear dimensions are in millimeters

RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Note D

4,80

4,30   2,60

1,50

2,55

2,05

0,85 X 16 PL.

0,28 X 16 PL.

10x0,50

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,75

4,25   2,65

1,50

0,82

1,07

0,30 x 2 PL

0,80 x 16 PL.

0,23 x 16 PL.

10x0,50

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,07

0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6xØ0,3

4208122−3/P 03/14
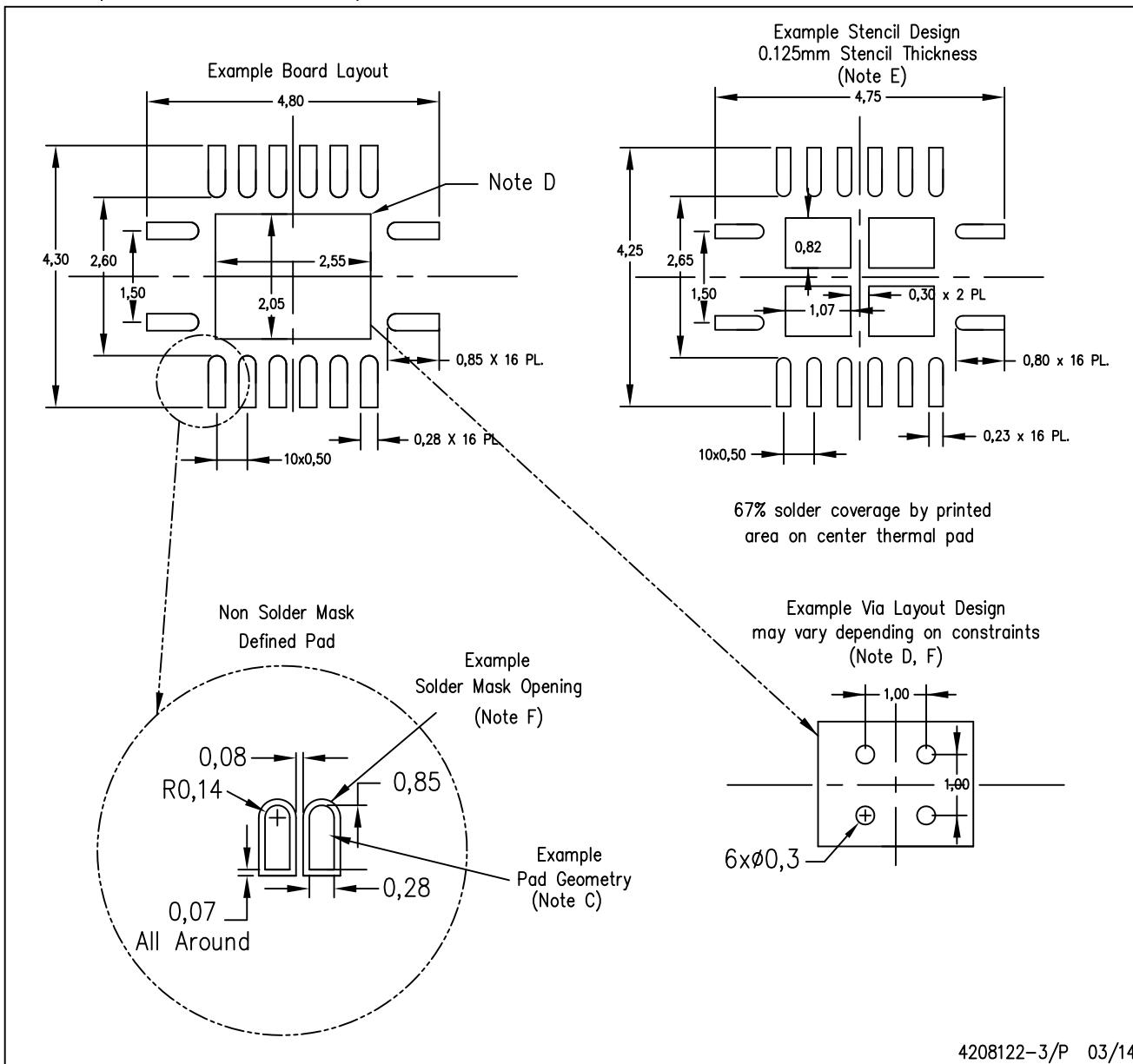
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

TEXAS
INSTRUMENTS
www.ti.com

DB (R-PDSO-G)** PLASTIC SMALL-OUTLINE

28 PINS SHOWN
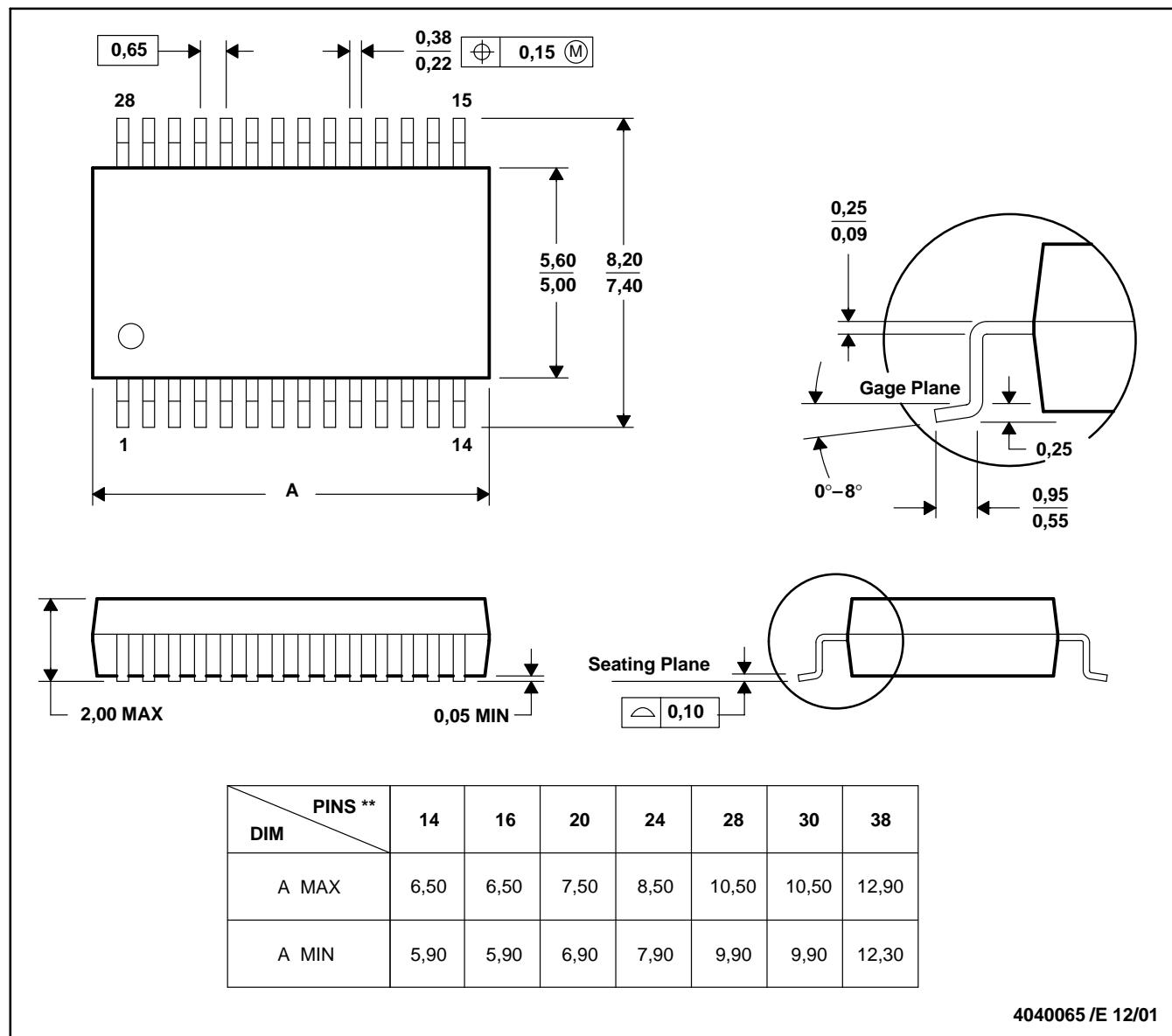
PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150