Product Change Notification

(Notification - P140312)

(CSTR2-T607)

March 21, 2014

To: *Our Valued Customer (Name)*

Overview: The purpose of this notification is to communicate product change of select Renesas Electronics America, Inc. (REA) devices. The following 4M-Bit LP SRAM series (3V) devices are transitioning from the current "D" version to a new generation "E" version. There are replacements devices available. The new "E" version is compatible form electrical characteristics specifications and package dimensions. Please see the Appendix for more information.

Current "D" Version	New "E" Version
R1LV0408D Series	RMLV0408E Series
R1LV0416D Series	RMLV0416E Series
R1LV0414D Series	RMLV0414E Series

Affected Products: A review of our shipment records to your company indicate the attached list of products is affected by this notification.

Booking Part Number	New Replacement Part Number
PN1	PN1a
PN2	PN2a
PN3	PN3a
PN4	PN4a

Part numbers given in this list are for active part numbers in REA database at the time of this notification.

Key Dates:

New generation "E" version of devices available	**Jun. 1st, 2014**
Final last time buy **(LTB)** orders placed to REA or to a franchised REA distributor for "D" version.	**Dec. 1st, 2015**
Planned date for last time shipment **(LTS)** from REA of "D" version.	**Jun. 15th, 2016**

Response: Please place last time buy (LTB) orders in a timely manner prior to the key dates listed to avoid product availability issues. If you anticipate volumes beyond your regular rate, please contact your REA sales representative with a forecast of your requirements. Shipments between the LTB and LTS dates are Non-Cancelable and Non-Returnable (NCNR).

You are encouraged to sample the new "E" version of the device and begin qualification as soon as possible. Please contact you REA sales representative to obtain samples.

Please contact your REA sales representative for any questions or comments.

Thank you for your attention.

Sincerely,

Renesas Electronics America, Inc.
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Appendix

Please note, the data in the tables below are accurate at time of notification release, however are subject to change.

Table 1: Device Comparison

EOL products (current "D" version)	PKG	Access time	Operation Temp.	Replacement products (new "E" version)	Access time	Operation Temp.
R1LV0408DSP-5SR	SOP (32)	55ns	0C to 70C	RMLV0408EGSP-4S2	45ns	-40C to 85C
R1LV0408DSP-5SI			-40C to 85C			
R1LV0408DSP-7LR		70ns	0C to70C			
R1LV0408DSP-7LI			-40C to 85C			
R1LV0408DSB-5SR	TSOP (32)	55ns	0C to 70C	RMLV0408EGSB-4S2		
R1LV0408DSB-5SI			-40C to 85C			
R1LV0408DSB-7LR		70ns	0C to 70C			
R1LV0408DSB-7LI			-40C to 85C			
R1LV0408DSA-5SR	sTSOP (32)	55ns	0C to 70C	RMLV0408EGSA-4S2		
R1LV0408DSA-5SI			-40C to 85C			
R1LV0408DSA-7LR		70ns	0C to 70C			
R1LV0408DSA-7LI			-40C to 85C			
R1LV0416DSB-5SI	TSOP (44) CS2pin	55ns	-40C to 85C	RMLV0416EGSB-4S2		
R1LV0416DSB-7LI		70ns				
R1LV0416DSD-5SK		55ns				
R1LV0414DSB-5SI	TSOP (44) CS1pin	55ns	-40C to 85C	RMLV0414EGSB-4S2		
R1LV0414DSB-7LI		70ns				
R1LV0416DBG-5SI	FBGA (48)	55ns	-40C to 85C	RMLV0416EGBG-4S2		
R1LV0416DBG-7LI		70ns				

Table 2: Assembly Comparison

Assembly	R1LV04**D*	RMLV04**E*
Resin material	Epoxy	Epoxy
Lead frame material	Fe-Ni 42 alloy	Cu
Lead frame plating	Sn/Cu	Sn
Inner wire material	Au	Au
Die bond material	Resin	Resin
Solder ball material for FBGA	Sn – Ag - Cu	Sn – Ag - Cu

Note: R1LV0416DSD-5SK Lead frame material is Cu. Lead frame plating is Sn.

Table 3: Moisture Comparison

Current "D" version	Moisture-proof performance	New "E" version	Moisture-proof performance
R1LV0408DSP	MS Level 2 Storage condition: 30C/70%RH 1year or less	RMLV0408EGSP	MS Level 3 Storage condition: 30C/70%RH 168h or less
R1LV0408DSB	MS Level 2 Storage condition: 30C/70%RH 1year or less	RMLV0408EGSB	MS Level 3 Storage condition: 30C/70%RH 168h or less
R1LV0408DSA	MS Level 2 Storage condition: 30C/70%RH 1year or less	RMLV0408EGSA	MS Level 3 Storage condition: 30C/70%RH 168h or less
R1LV0416DSB	MS Level 2 Storage condition: 30C/70%RH 1year or less	RMLV0416EGSB	MS Level 3 Storage condition: 30C/70%RH 168h or less
R1LV0416DSD	MS Level 3 Storage condition: 30C/70%RH 168h or less	RMLV0416EGSB	MS Level 3 Storage condition: 30C/70%RH 168h or less
R1LV0414DSB	MS Level 2 Storage condition: 30C/70%RH 1year or less	RMLV0414EGSB	MS Level 3 Storage condition: 30C/70%RH 168h or less
R1LV0416DBG	MS Level 3 Storage condition: 30C/70%RH 168h or less	RMLV0416EGBG	MS Level 3 Storage condition: 30C/70%RH 168h or less

Table 4: Characteristics Comparison

Item	Symbol	R1LV04**D series	Symbol	RMLV04**E series
Memory cell structure		TFT load + capacitor cell		<--
Peripheral circuit		CMOS		<--
Design rule		0.15um		0.11um
Package		SOP 32pin(20.75mm x 14.1mm)		<--
		TSOPII32pin(20.95mm x 11.76mm)		<--
		sTSOPI32pin(13.40mm x 8.00mm)		<--
		TSOPII44pin(18.41mm x 11.76mm)		<--
		FBGA 48ball(7.50mm x 8.50mm)		<--

DC condition

Item	Symbol	R1LV04**D series		Symbol	RMLV04**E series	
Supply voltage	Vcc	2.7V ~ 3.6V		Vcc	<--	
Operating temperature range	Ta	7LR/5SR	0 deg.C to 70 deg.C	Ta	-40 deg.C to 85 deg.C	
		7LI/5SI	-40 deg.C to 85 deg.C			
Input high voltage	VIH	2.2V(min.)/Vcc+0.3V(max.)		VIH	<--	
Input low voltage	VIL	-0.3V(min.)/0.6V(max.)		VIL	<--	

DC characteristics

Item	Symbol	R1LV04**D series		Symbol	RMLV04**E series	
Operating Current	Icc(CS1#=L, CS2=H, I I/O=0mA)	x8	10mA(max.)	Icc(CS1#=L, CS2=H, I I/O=0mA)	x8	<--
		x16	20mA(max.)		x16	10mA(max.)
	Icc1(TTL, Min.Cycle)	25mA(max.)		Icc1(TTL, Min.Cycle)	45ns cycle	<--
					55ns cycle	20mA(max.)
	Icc2(MOS, Cycle=1us)	5mA(max.)		Icc2(MOS, Cycle=1us)	2.5mA(max.)	
Stand by current	ISB(TTL)	0.3mA(max.)/0.1mA(typ.)		ISB(TTL)	<--	
	ISB1(MOS) 7LR/7LI	up to 25 deg.C	10uA(max.)/1.0uA(typ.)		-	
		up to 40 deg.C	10uA(max.)			
		up to 70 deg.C	16uA(max.)			
		up to 85 deg.C	20uA(max.)			
	ISB1(MOS) 5SR/5SI	up to 25 deg.C	2.5uA(max.)/1.0uA(typ.)	ISB1(MOS)	up to 25 deg.C	2.0uA(max.)/0.4uA(typ.)
		up to 40 deg.C	3uA(max.)		up to 40 deg.C	<--
		up to 70 deg.C	8uA(max.)		up to 70 deg.C	5uA(max.)
		up to 85 deg.C	10uA(max.)		up to 85 deg.C	7uA(max.)
Output high voltage	VOH	IOH=-1mA	2.4V(min.)	VOH	<--	
		IOH=-100uA	Vcc-0.2V		<--	
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	<--	
		IOL=100uA	0.2V(max.)		<--	

Capacitance

Item	Symbol	R1LV04**D series	Symbol	RMLV04**E series
Input capacitance	C in	8pF(max.)	C in	<--
Input/Output capacitance	C I/O	10pF(max.)	C I/O	<--

Data retention characteristics

Item	Symbol	R1LV04**D series		Symbol	RMLV04**E series	
Vcc for data retention	VDR	2.0V(min.)		VDR	1.5V(min.)	
Data retention current	IccDR(Vcc=3.0V) 7LR/7LI	up to 25 deg.C	10uA(max.)/1.0uA(typ.)	-	-	
		up to 40 deg.C	10uA(max.)			
		up to 70 deg.C	16uA(max.)			
		up to 85 deg.C	20uA(max.)			
	IccDR(Vcc=3.0V) 5SR/5SI	up to 25 deg.C	2.5uA(max.)/1.0uA(typ.)	IccDR(Vcc=3.0V)	up to 25 deg.C	2.0uA(max.)/0.4uA(typ.)
		up to 40 deg.C	3uA(max.)		up to 40 deg.C	<--
		up to 70 deg.C	8uA(max.)		up to 70 deg.C	5uA(max.)
		up to 85 deg.C	10uA(max.)		up to 85 deg.C	7uA(max.)
Chip deselect to data retention time	tCDR	0ns(min.)		tCDR	<--	
Operation recovery time	tR	5ms(min.)		tR	<--	

Table 4: Characteristics Comparison (cont.)

AC characteristics

Read Cycle

Item	Symbol	R1LV04**D series		Symbol	RMLV04**E series	
Read cycle time	tRC	-	-	tRC	4S2	45ns(min.)
		5SR/5SI	55ns(min.)		-	-
		7LR/7LI	70ns(min.)		-	-
Address access time	tAA	-	-	tAA	4S2	45ns(max.)
		5SR/5SI	55ns(max.)		-	-
		7LR/7LI	70ns(max.)		-	-
Chip select access time	tACS1/tACS2 tCO	-	-	tACS1/tACS2	4S2	45ns(max.)
		5SR/5SI	55ns(max.)		-	-
		7LR/7LI	70ns(max.)		-	-
Output enable to output valid	tOE	-	-	tOE	4S2	22ns(max.) : x16
						22ns(max.) : x8
		5SR/5SI	35ns(max.) : x16		-	-
		5SR/5SI	30ns(max.) : x8			
		7LR/7LI	40ns(max.) : x16		-	-
		7LR/7LI	35ns(max.) :x8			
Output hold from adress change	tOH	-	-	tOH	4S2	10ns(min.)
		5SR/5SI	10ns(min.)		-	-
		7LR/7LI	10ns(min.)		-	-
Chip select to output in low-Z	tCLZ1/tCLZ2	-	-	tCLZ1/tCLZ2/tCLZ	4S2	10ns(min.)
		5SR/5SI	10ns(min.)		-	-
		7LR/7LI	10ns(min.)		-	-
LB#, UB# disable to low-Z	tBLZ	-	-	tBLZ	4S2	5ns(min.)
		5SR/5SI	5ns(min.)		-	-
		7LR/7LI	5ns(min.)		-	-
Output enable to output in low-Z	tOLZ	-	-	tOLZ	4S2	5ns(min.)
		5SR/5SI	5ns(min.)		-	-
		7LR/7LI	5ns(min.)		-	-
Chip deselect to output in high-Z	tCHZ1/tCHZ2 tHZ	-	-	tCHZ1/tCHZ2/tCHZ	4S2	0ns(min.)/18ns(max.)
		5SR/5SI	0ns(min.)/20ns(max.)		-	-
		7LR/7LI	0ns(min.)/25ns(max.)		-	-
LB#, UB# disable to high-Z	tBHZ	-	-	tBHZ	4S2	0ns(min.)/18ns(max.)
		5SR/5SI	0ns(min.)/20ns(max.)		-	-
		7LR/7LI	0ns(min.)/25ns(max.)		-	-
Output disable to output in high-Z	tOHZ	-	-	tOHZ	4S2	0ns(min.)/18ns(max.)
		5SR/5SI	0ns(min.)/20ns(max.)		-	-
		7LR/7LI	0ns(min.)/25ns(max.)		-	-

Write Cycle

Item	Symbol	R1LV04**D series		Symbol	RMLV04**E series	
Write cycle time	tWC	-	-	tWC	4S2	45ns(min.)
		5SR/5SI	55ns(min.)		-	-
		7LR/7LI	70ns(min.)		-	-
Address valid to end of write	tAW	-	-	tAW	4S2	35ns(min.)
		5SR/5SI	50ns(min.)		-	-
		7LR/7LI	60ns(min.)		-	-
Chip select to end of write	tCW	-	-	tCW	4S2	35ns(min.)
		5SR/5SI	50ns(min.)		-	-
		7LR/7LI	60ns(min.)		-	-
Write pulse width	tWP	-	-	tWP	4S2	35ns(min.)
		5SR/5SI	40ns(min.)		-	-
		7LR/7LI	50ns(min.)		-	-
LB#, UB# valid to end of write	tBW	-	-	tBW	4S2	35ns(min.)
		5SR/5SI	50ns(min.)		-	-
		7LR/7LI	55ns(min.)		-	-
Address setup time	tAS	-	-	tAS	4S2	0ns(min.)
		5SR/5SI	0ns(min.)		-	-
		7LR/7LI	0ns(min.)		-	-
Write recovery time	tWR	-	-	tWR	4S2	0ns(min.)
		5SR/5SI	0ns(min.)		-	-
		7LR/7LI	0ns(min.)		-	-
Data to write time overlap	tDW	-	-	tDW	4S2	25ns(min.)
		5SR/5SI	25ns(min.)		-	-
		7LR/7LI	30ns(min.)		-	-
Data hold from write time	tDH	-	-	tDH	4S2	0ns(min.)
		5SR/5SI	0ns(min.)		-	-
		7LR/7LI	0ns(min.)		-	-
Output enable from end of write	tOW	-	-	tOW	4S2	5ns(min.)
		5SR/5SI	5ns(min.)		-	-
		7LR/7LI	5ns(min.)		-	-
Output disable to output in high-Z	tOHZ	-	-	tOHZ	4S2	0ns(min.)/18ns(max.)
		5SR/5SI	0ns(min.)/20ns(max.)		-	-
		7LR/7LI	0ns(min.)/25ns(max.)		-	-
Write to output in high-Z	tWHZ	-	-	tWHZ	4S2	0ns(min.)/18ns(max.)
		5SR/5SI	0ns(min.)/20ns(max.)		-	-
		7LR/7LI	0ns(min.)/25ns(max.)		-	-