



Low-Power, Rail-to-Rail Output, 16-Bit Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **microPOWER OPERATION:** 250µA at 5V
- **MULTIPLYING-MODE BANDWIDTH:** 350kHz
- **POWER-ON RESET TO ZERO**
- **POWER SUPPLY:** +2.7V to +5.5V
- **ENSURED MONOTONIC BY DESIGN**
- **SETTLING TIME:** 10µs to ±0.003% FSR
- **LOW-POWER SERIAL INTERFACE WITH SCHMITT-TRIGGERED INPUTS**
- **ON-CHIP OUTPUT BUFFER AMPLIFIER, RAIL-TO-RAIL OPERATION**
- **SYNC INTERRUPT FACILITY**
- **MSOP-8 PACKAGE**

APPLICATIONS

- **PROCESS CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **CLOSED-LOOP SERVO-CONTROL**
- **PC PERIPHERALS**
- **PORTABLE INSTRUMENTATION**
- **PROGRAMMABLE ATTENUATION**

DESCRIPTION

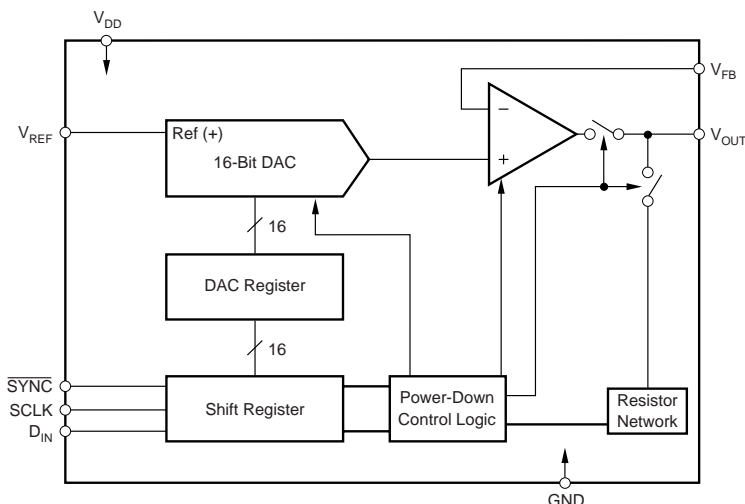
The DAC8501 is a low-power, single, 16-bit buffered voltage output Digital-to-Analog Converter (DAC) optimized for multiplying operation. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC8501 uses a versatile 3-wire serial interface that operates at clock rates up to 30MHz and is compatible with standard SPI™, QSPI™, Microwire™, and Digital Signal Processor (DSP) interfaces.

The DAC8501 requires an external reference voltage to set the output range of the DAC. The DAC8501 incorporates a power-on reset circuit that ensures that the DAC output powers up at 0V and remains there until a valid write takes place to the device. The DAC8501 contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 200nA at 5V.

The low-power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The power consumption is 1.2mW at 5V reducing to 1µW in power-down mode.

The DAC8501 is available in an MSOP-8 package.

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Microwire is a registered trademark of National Semiconductor.



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V_{DD} to GND	-0.3V to +6V
Digital Input Voltage to GND	-0.3V to $+V_{DD} + 0.3V$
V_{OUT} to GND	-0.3V to $+V_{DD} + 0.3V$
V_{REF} to GND	-0.3V to $+V_{DD} + 0.3V$
V_{FB} to GND	-0.3V to $+V_{DD} + 0.3V$
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature Range (T_J max)	+150°C
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering:	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

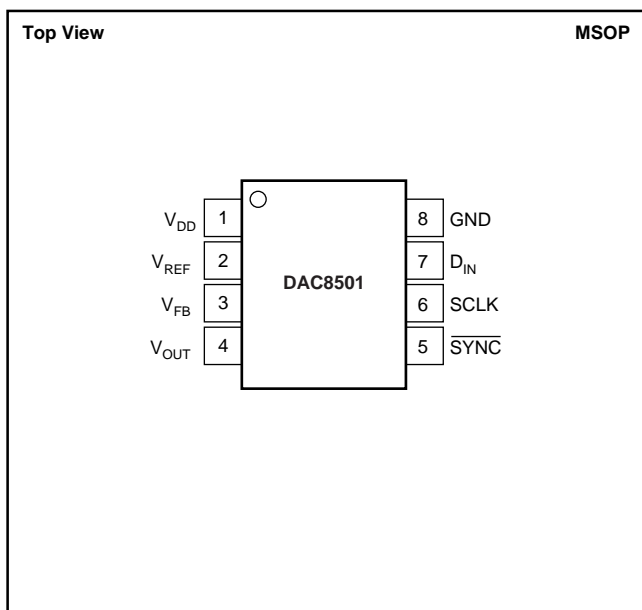
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8501E "	±64 "	±1 "	MSOP-8 "	DGK "	-40°C to +105°C "	D01 "	DAC8501E/250 DAC8501E/2K5	Tape and Reel, 250 Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	V_{DD}	Power-Supply Input, +2.7V to +5.5V
2	V_{REF}	Reference Voltage Input
3	V_{FB}	Feedback connection for the output amplifier.
4	V_{OUT}	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
5	\overline{SYNC}	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When \overline{SYNC} goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless \overline{SYNC} is taken HIGH before this edge, in which case the rising edge of \overline{SYNC} acts as an interrupt and the write sequence is ignored by the DAC8501.
6	SCLK	Serial Clock Input. Data can be transferred at rates up to 30MHz.
7	D_{IN}	Serial Data Input. Data is clocked into the 24-bit input shift register on the falling edge of the serial clock input.
8	GND	Ground reference point for all circuitry on the part.

ELECTRICAL CHARACTERISTICS

$V_{DD} = +2.7V$ to $+5.5V$, and $-40^{\circ}C$ to $+105^{\circ}C$, unless otherwise specified.

PARAMETER	CONDITIONS	DAC8501E			UNITS
		MIN	TYP	MAX	
STATIC PERFORMANCE⁽¹⁾ Resolution Relative Accuracy Differential Nonlinearity Zero Code Error Full-Scale Error Gain Error Zero Code Error Drift Gain Temperature Coefficient	Ensured Monotonic by Design All Zeroes Loaded to DAC Register All Ones Loaded to DAC Register	16	+5 -0.15	± 0.098 ± 1 ± 20 ± 1.25 ± 1.25	Bits % of FSR LSB mV % of FSR % of FSR $\mu V/^{\circ}C$ ppm of FSR/ $^{\circ}C$
OUTPUT CHARACTERISTICS⁽²⁾ Output Voltage Range Output Voltage Settling Time Slew Rate Capacitive Load Stability Code Change Glitch Impulse Digital Feedthrough DC Output Impedance Short-Circuit Current Power-Up Time	To $\pm 0.003\%$ FSR 0200 _H to FD00 _H $R_L = 2k\Omega$; $0pF < C_L < 200pF$ $R_L = 2k\Omega$; $C_L = 500pF$ $R_L = \infty$ $R_L = 2k\Omega$ to Ground 1LSB Change Around Major Carry $V_{DD} = +5V$ $V_{DD} = +3V$ Coming Out of Power-Down Mode $V_{DD} = +5V$ Coming Out of Power-Down Mode $V_{DD} = +3V$	0	8 12 1 470 1000 20 0.5 1 50 20 2.5 5	V_{REF} 10 V/ μs pF pF nV-s Ω mA mA μs μs	V μs μs pF pF nV-s nV-s Ω mA mA μs μs
REFERENCE INPUT Reference Current Reference Input Range Reference Input Impedance	$V_{REF} = V_{DD} = +5V$ $V_{REF} = V_{DD} = +3.6V$	0	35 20 150	45 30 V_{DD}	μA μA V k Ω
MULTIPLYING MODE Small-Signal Bandwidth Full-Power Bandwidth			350 64		kHz kHz
LOGIC INPUTS⁽²⁾ Input Current V_{INL} , Input LOW Voltage V_{INL} , Input LOW Voltage V_{INH} , Input HIGH Voltage V_{INH} , Input HIGH Voltage Pin Capacitance	$V_{DD} = +5V$ $V_{DD} = +3V$ $V_{DD} = +5V$ $V_{DD} = +3V$	2.4 2.1		± 1 0.8 0.6 3	μA V V V pF
POWER REQUIREMENTS V_{DD} I_{DD} (normal mode) $V_{DD} = +3.6V$ to $+5.5V$ $V_{DD} = +2.7V$ to $+3.6V$ I_{DD} (all power-down modes) $V_{DD} = +3.6V$ to $+5.5V$ $V_{DD} = +2.7V$ to $+3.6V$	DAC Active and Excluding Load Current $V_{IH} = V_{DD}$ and $V_{IL} = GND$ $V_{IH} = V_{DD}$ and $V_{IL} = GND$ $V_{IH} = V_{DD}$ and $V_{IL} = GND$ $V_{IH} = V_{DD}$ and $V_{IL} = GND$	2.7	250 240 0.2 0.05	5.5 400 390 1 1	V μA μA μA μA
POWER EFFICIENCY I_{OUT}/I_{DD}	$I_{LOAD} = 2mA$, $V_{DD} = +5V$		89		%
TEMPERATURE RANGE Specified Performance		-40		+105	$^{\circ}C$

NOTES: (1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded. (2) Ensured by design and characterization, not production tested.

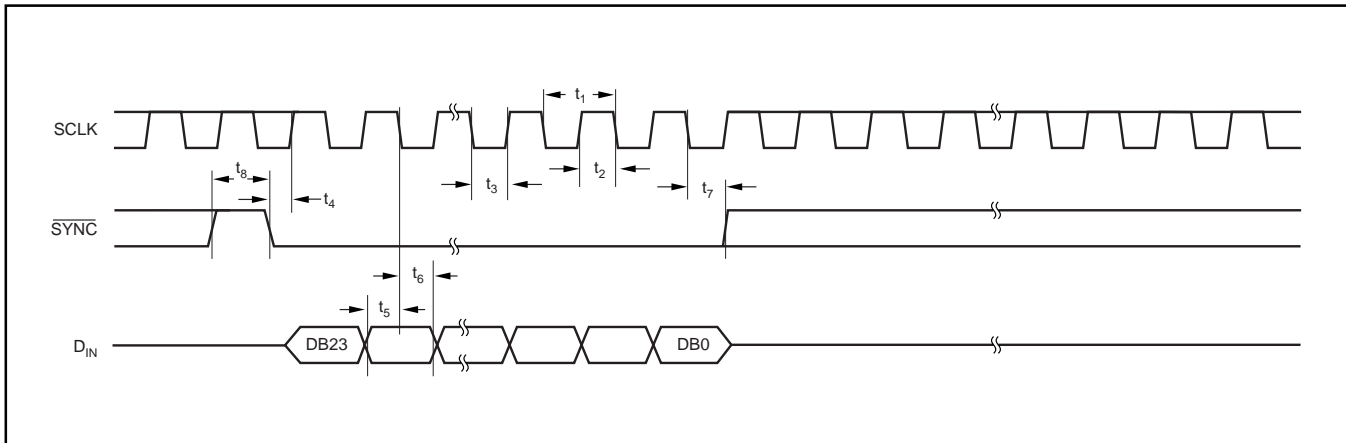
TIMING CHARACTERISTICS(1, 2)

$V_{DD} = +2.7V$ to $+5.5V$; all specifications $-40^{\circ}C$ to $+105^{\circ}C$, unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	DAC8501E			UNITS
			MIN	TYP	MAX	
$t_1^{(3)}$	SCLK Cycle Time	$V_{DD} = 2.7V$ to $3.6V$ $V_{DD} = 3.6V$ to $5.5V$	50 33			ns ns
t_2	SCLK HIGH Time	$V_{DD} = 2.7V$ to $3.6V$ $V_{DD} = 3.6V$ to $5.5V$	13 13			ns ns
t_3	SCLK LOW Time	$V_{DD} = 2.7V$ to $3.6V$ $V_{DD} = 3.6V$ to $5.5V$	22.5 13			ns ns
t_4	\overline{SYNC} to SCLK Rising Edge Setup Time	$V_{DD} = 2.7V$ to $3.6V$ $V_{DD} = 3.6V$ to $5.5V$	0 0			ns ns
t_5	Data Setup Time	$V_{DD} = 2.7V$ to $3.6V$ $V_{DD} = 3.6V$ to $5.5V$	5 5			ns ns
t_6	Data Hold Time	$V_{DD} = 2.7V$ to $3.6V$ $V_{DD} = 3.6V$ to $5.5V$	4.5 4.5			ns ns
t_7	SCLK Falling Edge to \overline{SYNC} Rising Edge	$V_{DD} = 2.7V$ to $3.6V$ $V_{DD} = 3.6V$ to $5.5V$	0 0			ns ns
t_8	Minimum \overline{SYNC} HIGH Time	$V_{DD} = 2.7V$ to $3.6V$ $V_{DD} = 3.6V$ to $5.5V$	50 33			ns ns

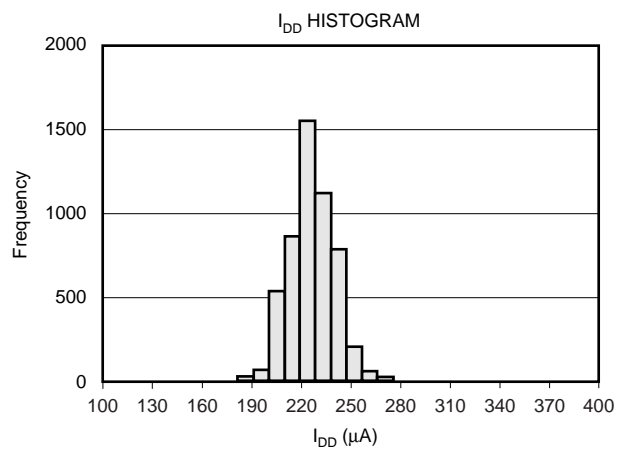
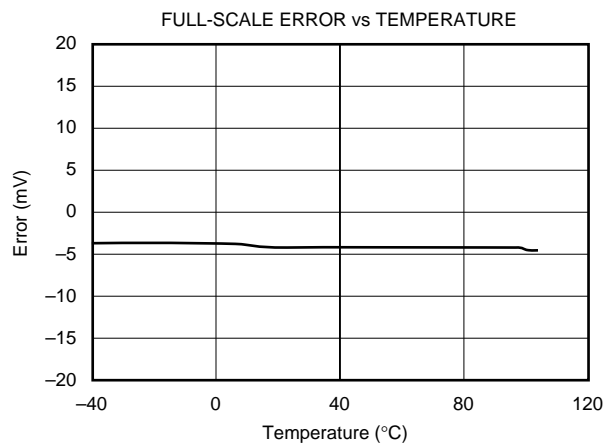
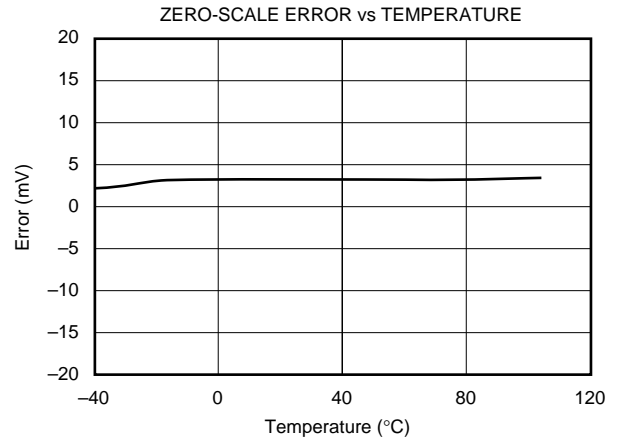
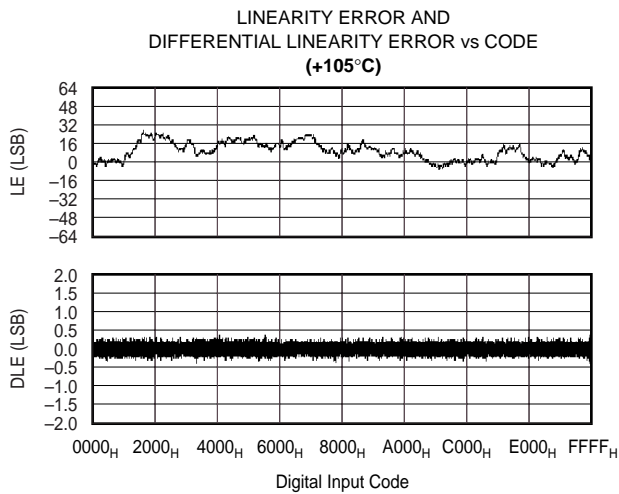
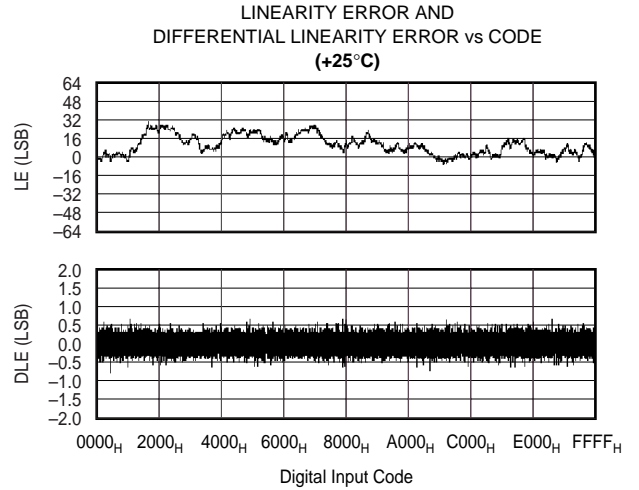
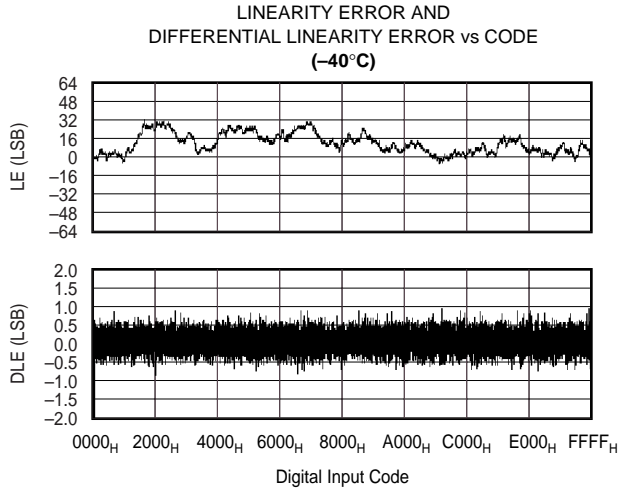
NOTES: (1) All input signals are specified with $t_R = t_F = 5ns$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (2) See Serial Write Operation timing diagram, below. (3) Maximum SCLK frequency is 30MHz at $V_{DD} = +3.6V$ to $+5.5V$ and 20MHz at $V_{DD} = +2.7V$ to $+3.6V$.

SERIAL WRITE OPERATION



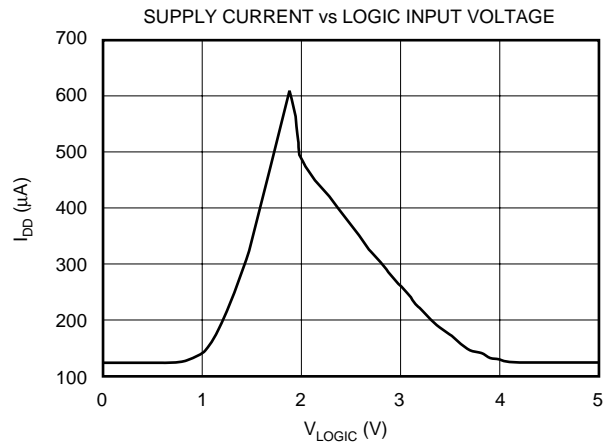
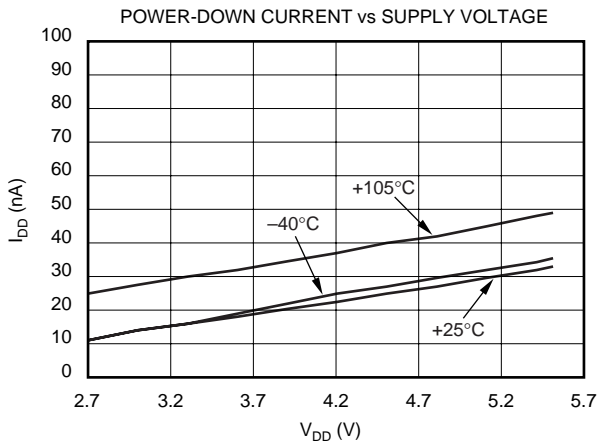
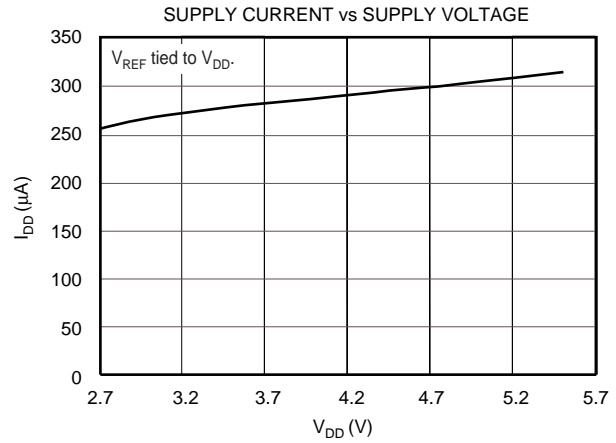
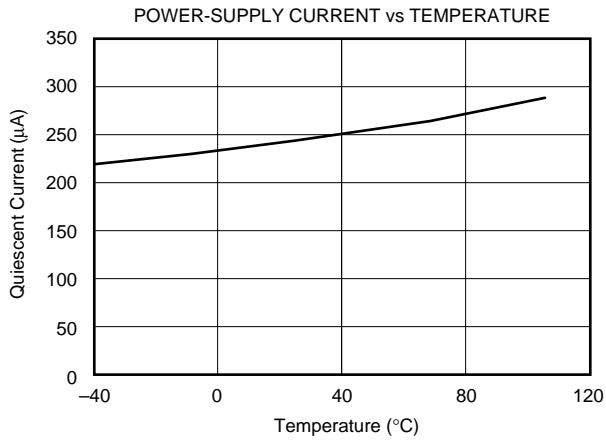
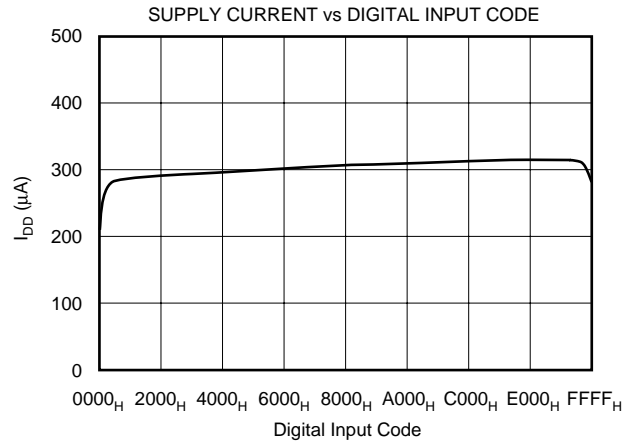
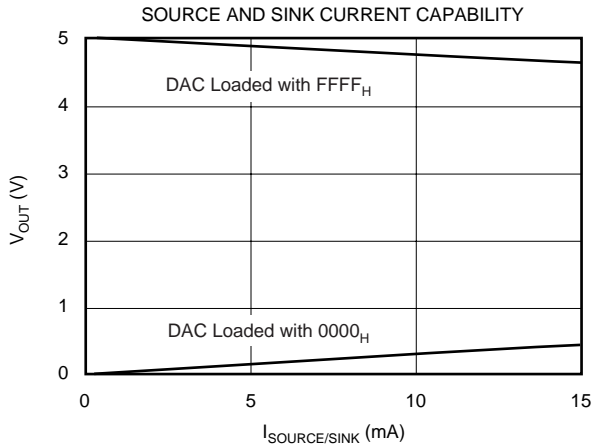
TYPICAL CHARACTERISTICS: $V_{DD} = +5V$

At $T_A = +25^\circ\text{C}$, and $+V_{DD} = +5V$, unless otherwise noted.



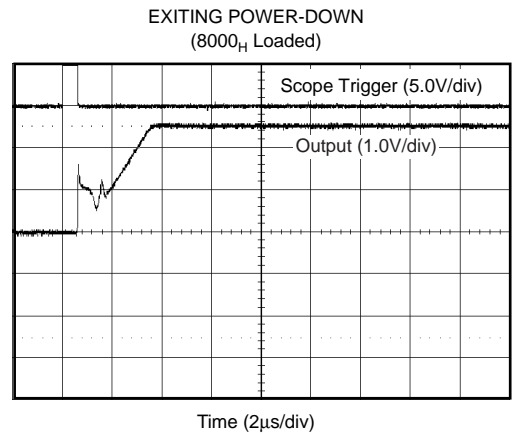
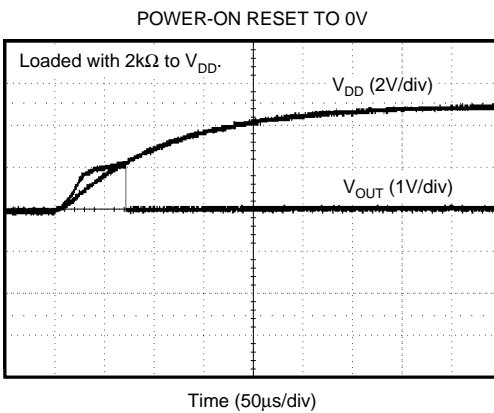
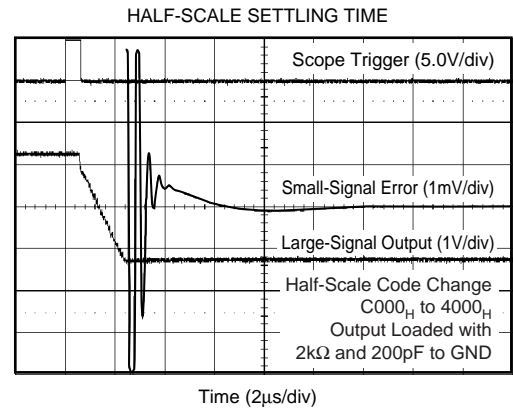
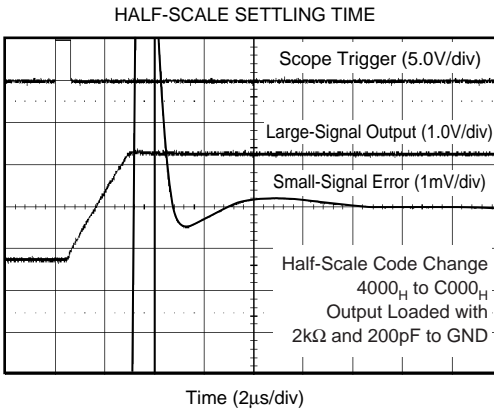
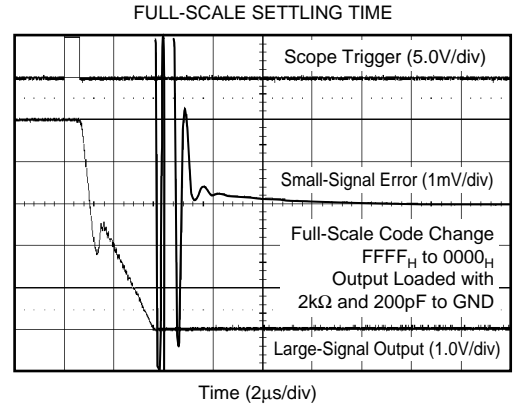
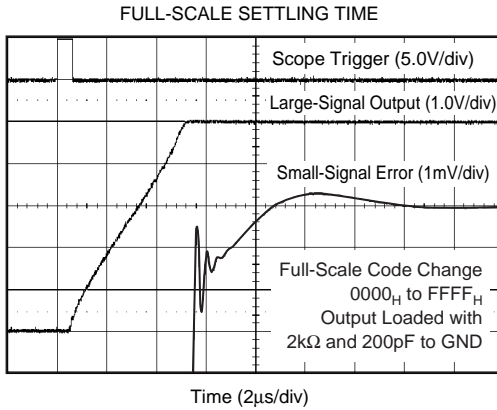
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At $T_A = +25^\circ\text{C}$, and $+V_{DD} = +5V$, unless otherwise noted.



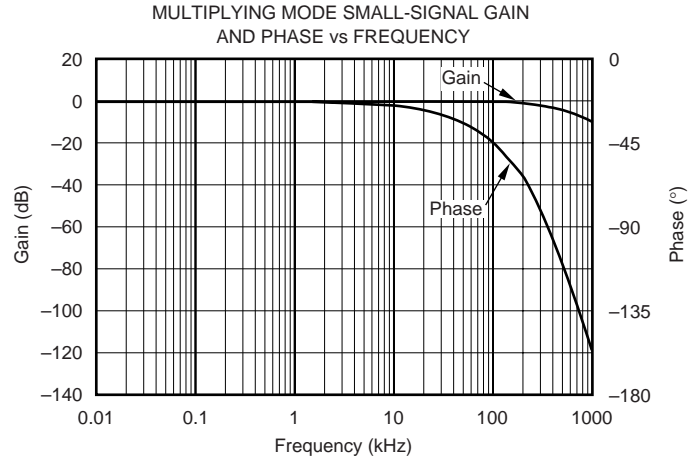
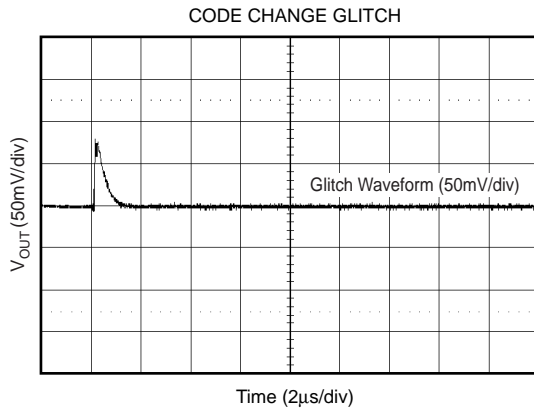
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At $T_A = +25^\circ C$, and $+V_{DD} = +5V$, unless otherwise noted.



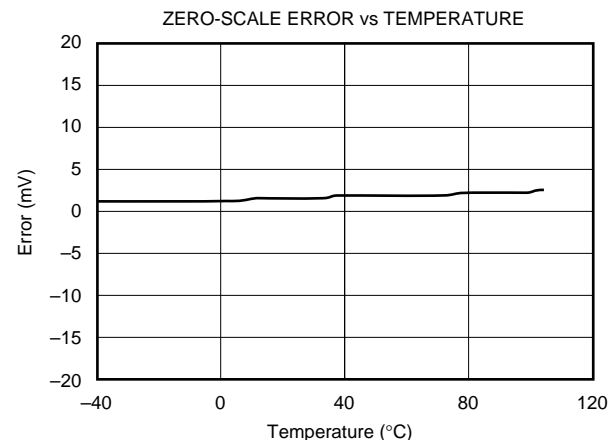
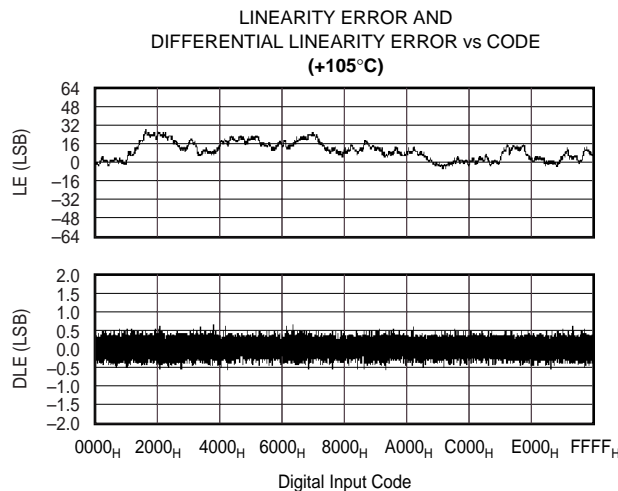
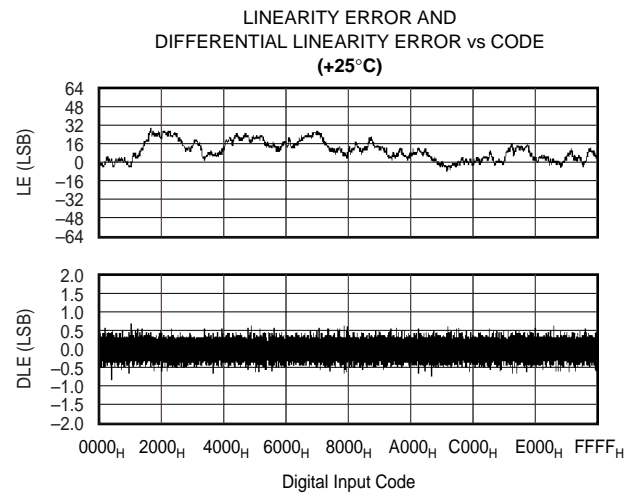
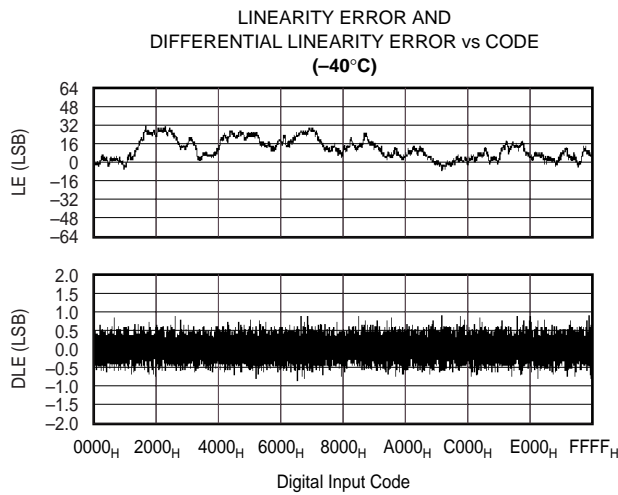
TYPICAL CHARACTERISTICS: $V_{DD} = +5V$ (Cont.)

At $T_A = +25^\circ\text{C}$, and $+V_{DD} = +5V$, unless otherwise noted.



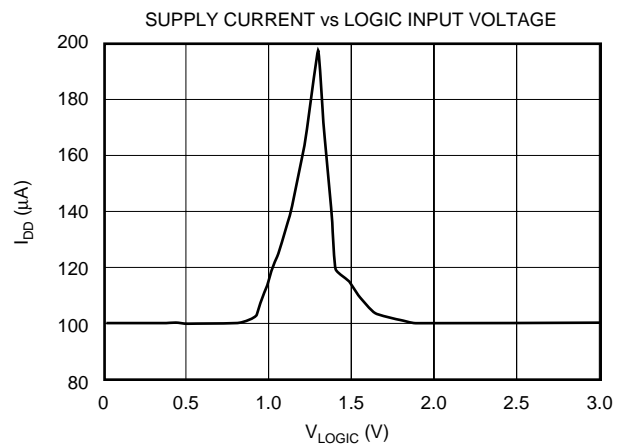
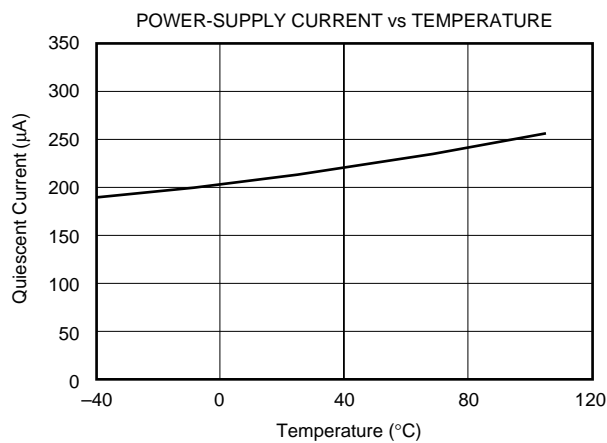
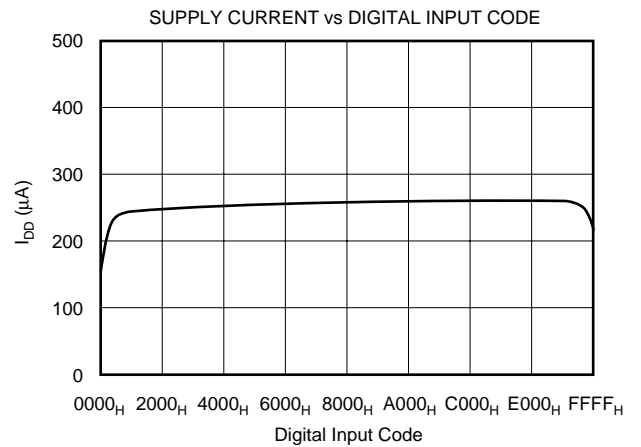
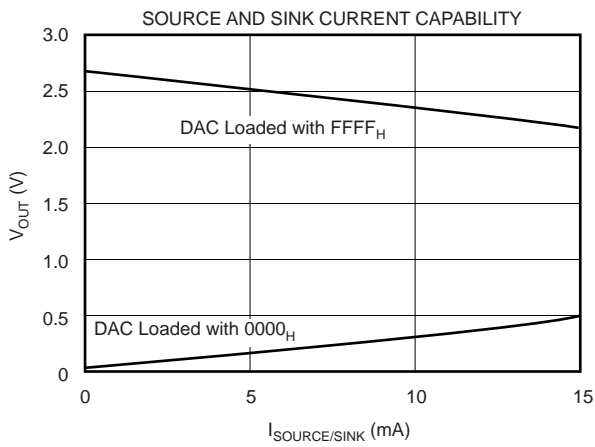
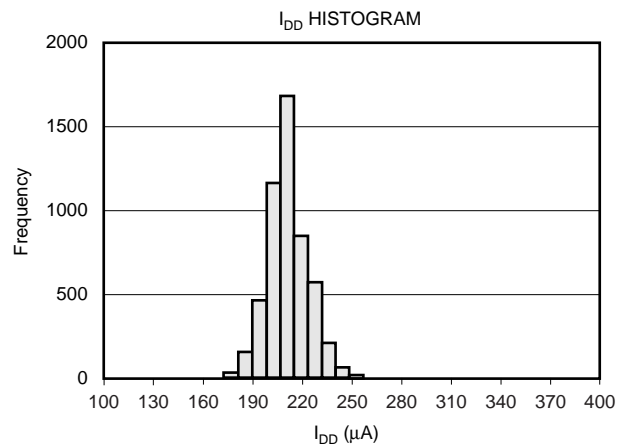
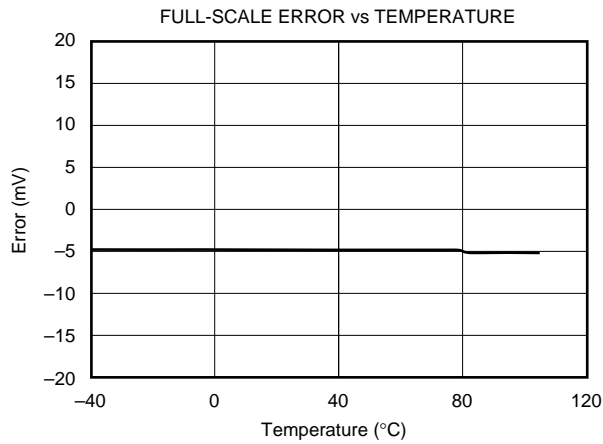
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At $T_A = +25^\circ\text{C}$, and $+V_{DD} = +2.7V$, unless otherwise noted.



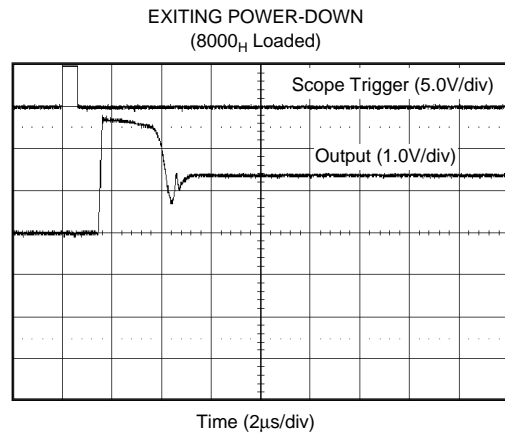
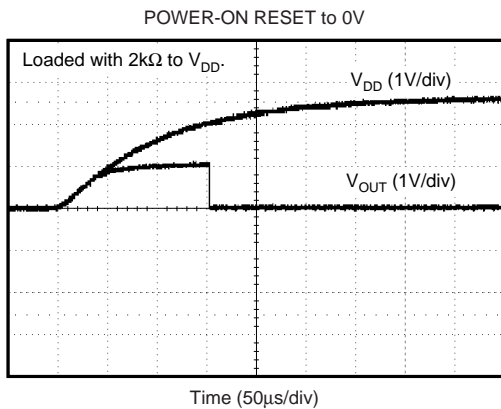
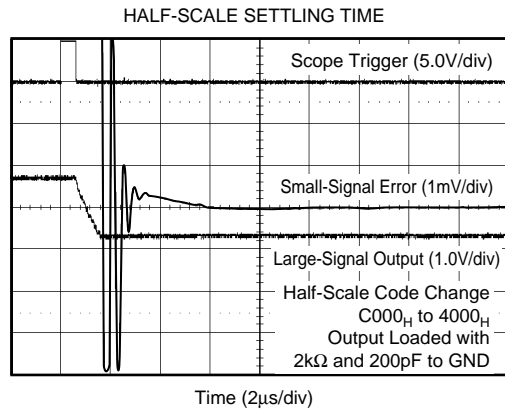
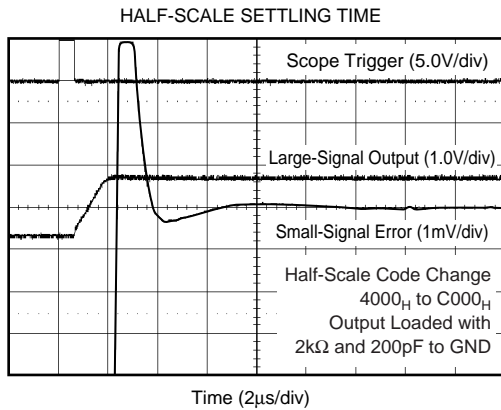
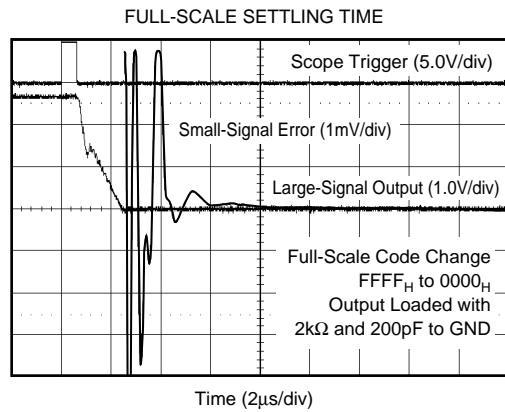
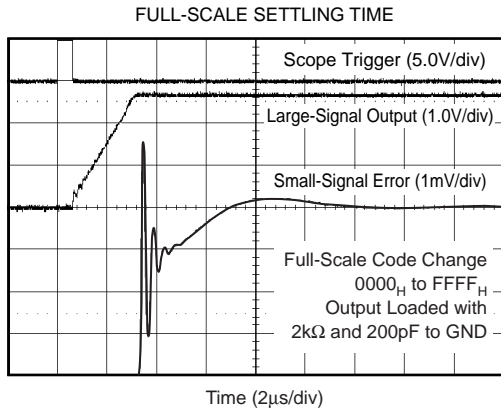
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At $T_A = +25^\circ C$, and $+V_{DD} = +2.7V$, unless otherwise noted.



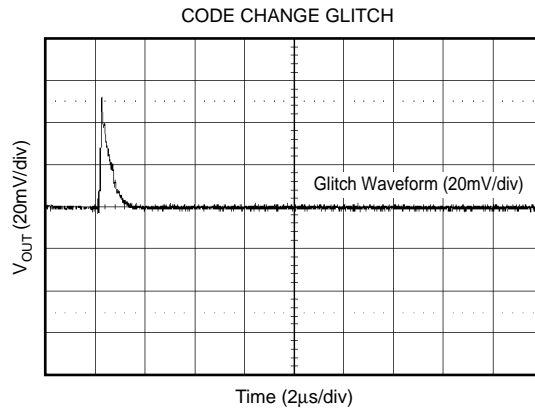
TYPICAL CHARACTERISTICS: $V_{DD} = +2.7V$ (Cont.)

At $T_A = +25^\circ C$, and $+V_{DD} = +2.7V$, unless otherwise noted.



TYPICAL CHARACTERISTICS: $V_{DD} = +2.7V$ (Cont.)

At $T_A = +25^\circ C$, and $+V_{DD} = +2.7V$, unless otherwise noted.



THEORY OF OPERATION

DAC SECTION

The architecture consists of a string DAC followed by an output buffer amplifier. Figure 1 shows a block diagram of the DAC architecture.

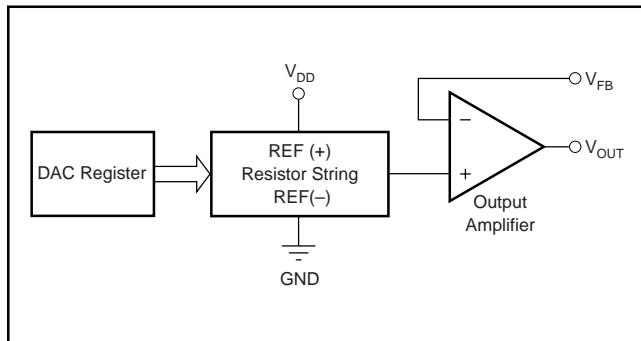


FIGURE 1. DAC8501 Architecture.

The input coding to the DAC8501 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = V_{REF} \cdot \frac{D}{65536} \quad (1)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

The resistor string section is shown in Figure 2, it is simply a string of resistors, each of value R . The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is ensured monotonic because it is a string of resistors.

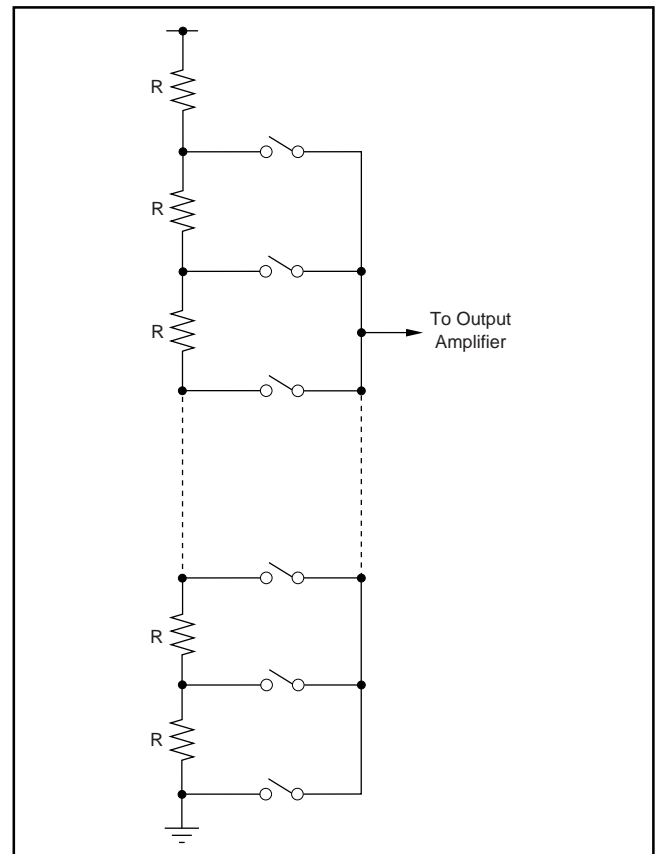


FIGURE 2. Resistor String.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0V to V_{DD} ; it is capable of driving a load of $2k\Omega$ in parallel with $1000pF$ to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics. The slew rate is $1V/\mu s$ with a full-scale settling time of $8\mu s$ with the output unloaded.

The inverting input of the output amplifier is brought out to the V_{FB} pin which allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

MULTIPLYING MODE OPTIMIZATIONS

The DAC8501 is a version of the DAC8531 optimized for multiplying mode at a typical bandwidth of up to $350kHz$, which gives better phase and gain performance.

Two aspects of the DAC8501 operation are affected by the optimizations. The resistor string in the DAC8531 is disconnected from the reference input when power-down mode is entered, but in the DAC8501, the resistor string continues to draw current from the reference input during power-down mode.

The DAC8501 has slightly different offset characteristics from the DAC8531: the DAC8501 may output 0V for the first few hundred codes, whereas the DAC8531 typically has far fewer such dead codes near 0. Offset and gain errors are measured from code 0200_H for both devices, so specifications are not affected. In all other respects, the DAC8531 and DAC8501 operate identically.

Multiplying-mode bandwidth is measured at both small-signal and full-power levels. Bandwidth at full-power amplitude, which is typically $64kHz$, is limited by the $1V/\mu s$ slew rate of the output amplifier. Small-amplitude signals that do not cause the amplifier to slew are bandlimited by the output amplifier to approximately $350kHz$. If the design approaches either of these limits, the DAC8501 must be tested in the application to ensure that it meets the needed requirements.

SERIAL INTERFACE

The DAC8501 has a 3-wire serial interface (\overline{SYNC} , SCLK, and D_{IN}), which is compatible with SPI, QSPI, and Microwire interface standards as well as most DSPs, (see the Serial Write Operation timing diagram for an example of a typical write sequence).

The write sequence begins by bringing the \overline{SYNC} line LOW, data from the D_{IN} line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as $30MHz$, making the DAC8501 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed (i.e., a change in DAC register contents and/or a change in the mode of operation).

At this point, the \overline{SYNC} line can be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of $33ns$ before the next write sequence so that a falling edge of \overline{SYNC} can initiate the next write sequence. As the \overline{SYNC} buffer draws more current when the \overline{SYNC} signal is HIGH than it does when it is LOW, \overline{SYNC} must be idled LOW between write sequences for lowest power operation of the part; as mentioned above, it must be brought HIGH again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide, as shown in Figure 3. The first six bits are *don't cares*. The next two bits (PD1 and PD0) are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes): there is a more complete description of the various modes in the Power-Down Modes section. The next 16 bits are the data bits which are transferred to the DAC register on the 24th falling edge of SCLK.

SYNC INTERRUPT

In a normal write sequence, the \overline{SYNC} line is kept LOW for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if \overline{SYNC} is brought HIGH before the 24th falling edge, this acts as an interrupt to the write sequence. When this happens, the shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs, as shown in Figure 4.



FIGURE 3. Data Input Register.

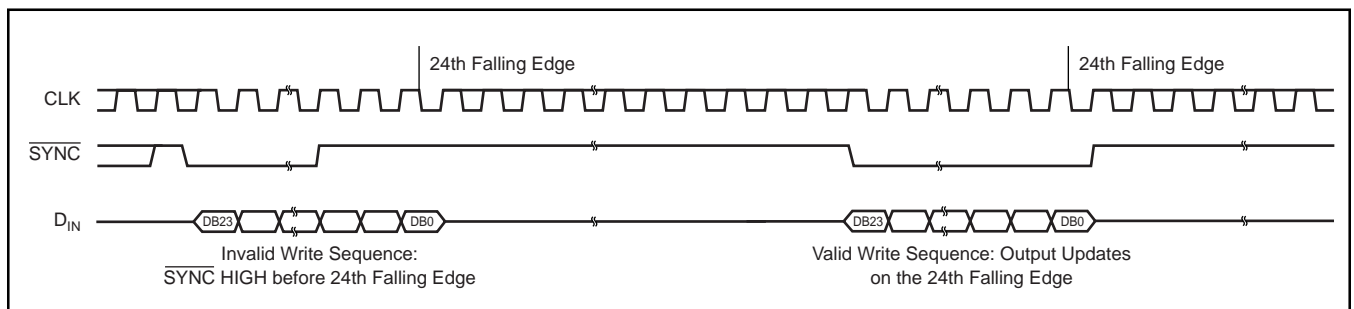


FIGURE 4. \overline{SYNC} Interrupt Facility.

POWER-ON RESET

The DAC8501 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0V; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC when it is in the process of powering up.

POWER-DOWN MODES

The DAC8501 supports four separate modes of operation which are programmable by setting two bits (PD1 and PD0) in the control register. Table I shows how the state of the bits corresponds to the mode of operation of the device.

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal Operation
—	—	Power-Down Modes
0	1	Output 1kΩ to GND
1	0	Output 100kΩ to GND
1	1	High-Z

TABLE I. Modes of Operation for the DAC8501.

When both bits are set to 0, the part works normally with its typical current consumption of 250μA at 5V; however, for the three power-down modes, the supply current falls to 200nA at 5V (50nA at 3V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values, this has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options: the output is connected internally to GND through a 1kΩ resistor; a 100kΩ resistor; or it is left open-circuited (High-Z), Figure 5 shows the output stage.

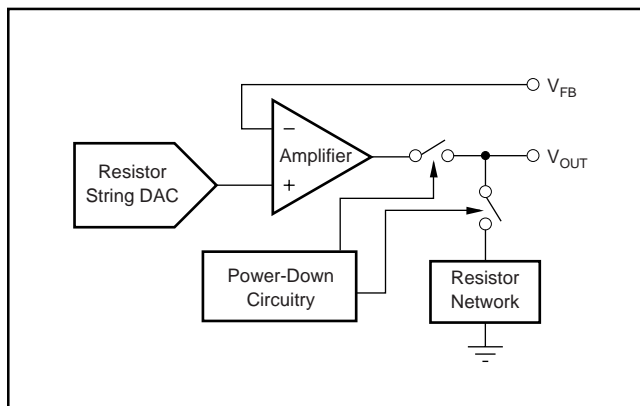


FIGURE 5. Output Stage During Power-Down.

All linear circuitry is shut down when the power-down mode is activated, however, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5μs for $V_{DD} = 5V$, and 5μs for $V_{DD} = 3V$, (see the Typical Characteristics for more information).

MICROPROCESSOR INTERFACING

DAC8501 TO 8051 INTERFACE

Figure 6 shows a serial interface between the DAC8501 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8501, whereas RXD drives the serial data line of the part. The SYNC signal is derived from a bit-programmable pin on the port, in this case, port line P3.3 is used. When data is to be transmitted to the DAC8501, P3.3 is taken LOW. The 8051 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which has the LSB first. The DAC8501 requires its data with the MSB as the first bit received, therefore the 8051 transmit routine must take this into account, and mirror the data as needed.

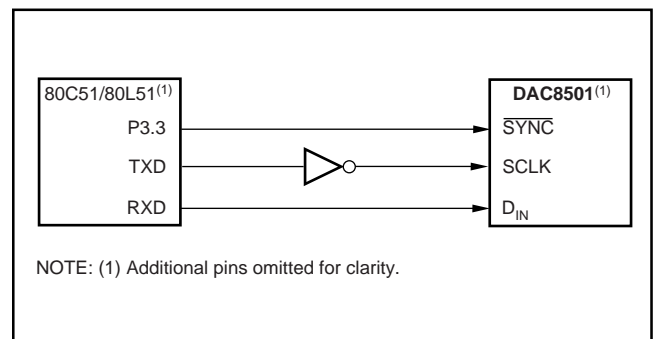


FIGURE 6. DAC8501 to 80C51/80L51 Interface.

DAC8501 TO Microwire INTERFACE

Figure 7 shows an interface between the DAC8501 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8501 on the rising edge of the SK signal.

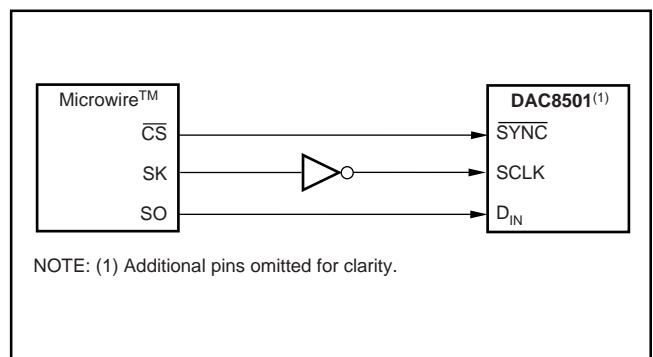


FIGURE 7. DAC8501 to Microwire Interface.

DAC8501 TO 68HC11 INTERFACE

Figure 8 shows a serial interface between the DAC8501 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8501, whereas the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7), similar to what was done for the 8051.

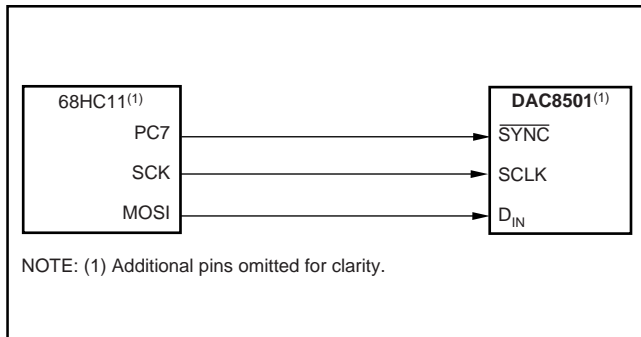


FIGURE 8. DAC8501 to 68HC11 Interface.

The 68HC11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1, this configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle, data is transmitted MSB first. In order to load data to the DAC8501, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC and PC7 is taken HIGH at the end of this procedure.

APPLICATIONS

USING REF02 AS A POWER SUPPLY FOR THE DAC8501

Due to the extremely low supply current required by the DAC8501, an alternative option is to use a REF02 +5V precision voltage reference to supply the required voltage to the part, as shown in Figure 9. This is especially useful if the power supply is quite noisy or if the system supply voltages

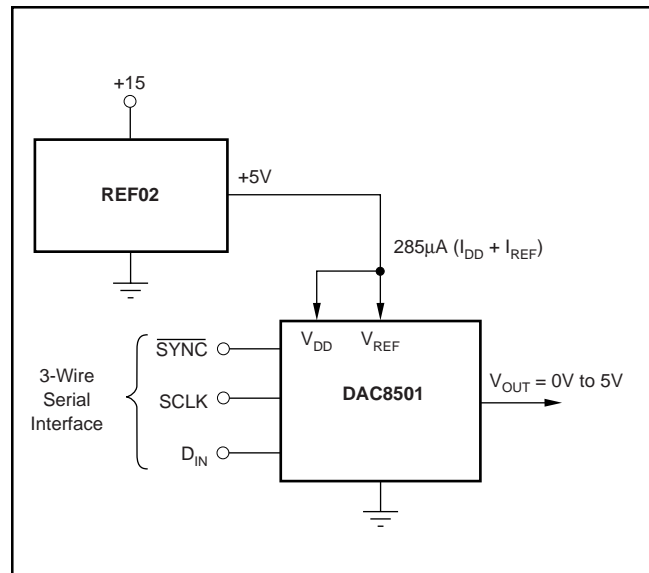


FIGURE 9. REF02 as a Power Supply to the DAC8501.

are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC8501; if the REF02 is used, the typical current it needs to supply to the DAC8501 is $285\mu\text{A}$. This is with no load on the output of the DAC. When the DAC output is loaded, the REF02 also needs to supply the current to the load. The total current required (with a $5\text{k}\Omega$ load on the DAC output) is:

$$285\mu\text{A} + (5\text{V}/5\text{k}\Omega) = 1.29\text{mA} \quad (2)$$

The load regulation of the REF02 is typically $0.005\%/ \text{mA}$, which results in an error of $322\mu\text{V}$ for the 1.29mA current drawn from it. This corresponds to a 4.2LSB error.

BIPOLAR OPERATION USING THE DAC8501

The DAC8501 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 10. The circuit shown will give an output voltage range of $\pm V_{\text{REF}}$. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

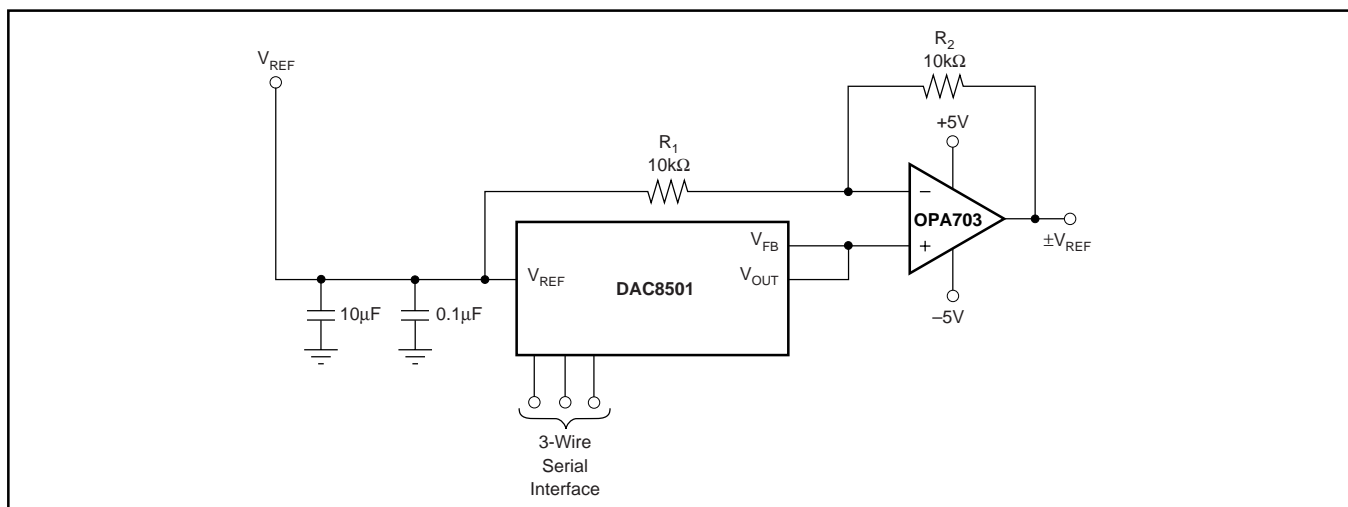


FIGURE 10. Bipolar Operation with the DAC8501.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{REF} \cdot \left(\frac{D}{65536} \right) \cdot \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \cdot \left(\frac{R_2}{R_1} \right) \right] \quad (3)$$

where D represents the input code in decimal (0 to 65535). With $V_{REF} = 5V$, $R_1 = R_2 = 10k\Omega$:

$$V_O = \left(\frac{10 \cdot D}{65536} \right) - 5V \quad (4)$$

This is an output voltage range of $\pm 5V$ with 0000_H corresponding to a $-5V$ output and $FFFF_H$ corresponding to a $+5V$ output. Similarly, using $V_{REF} = 2.5V$, a $\pm 2.5V$ output voltage range can be achieved.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

As the DAC8501 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to keep digital noise from appearing at the output.

Due to the single ground pin of the DAC8501, all return currents, including digital and analog return currents, must flow through the GND pin, which would, ideally, be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, the $1\mu F$ to $10\mu F$ and $0.1\mu F$ bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a $100\mu F$ electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the $+5V$ supply, removing the high-frequency noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8501E/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D01	Samples
DAC8501E/250G4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D01	Samples
DAC8501E/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D01	Samples
DAC8501E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D01	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8501E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8501E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

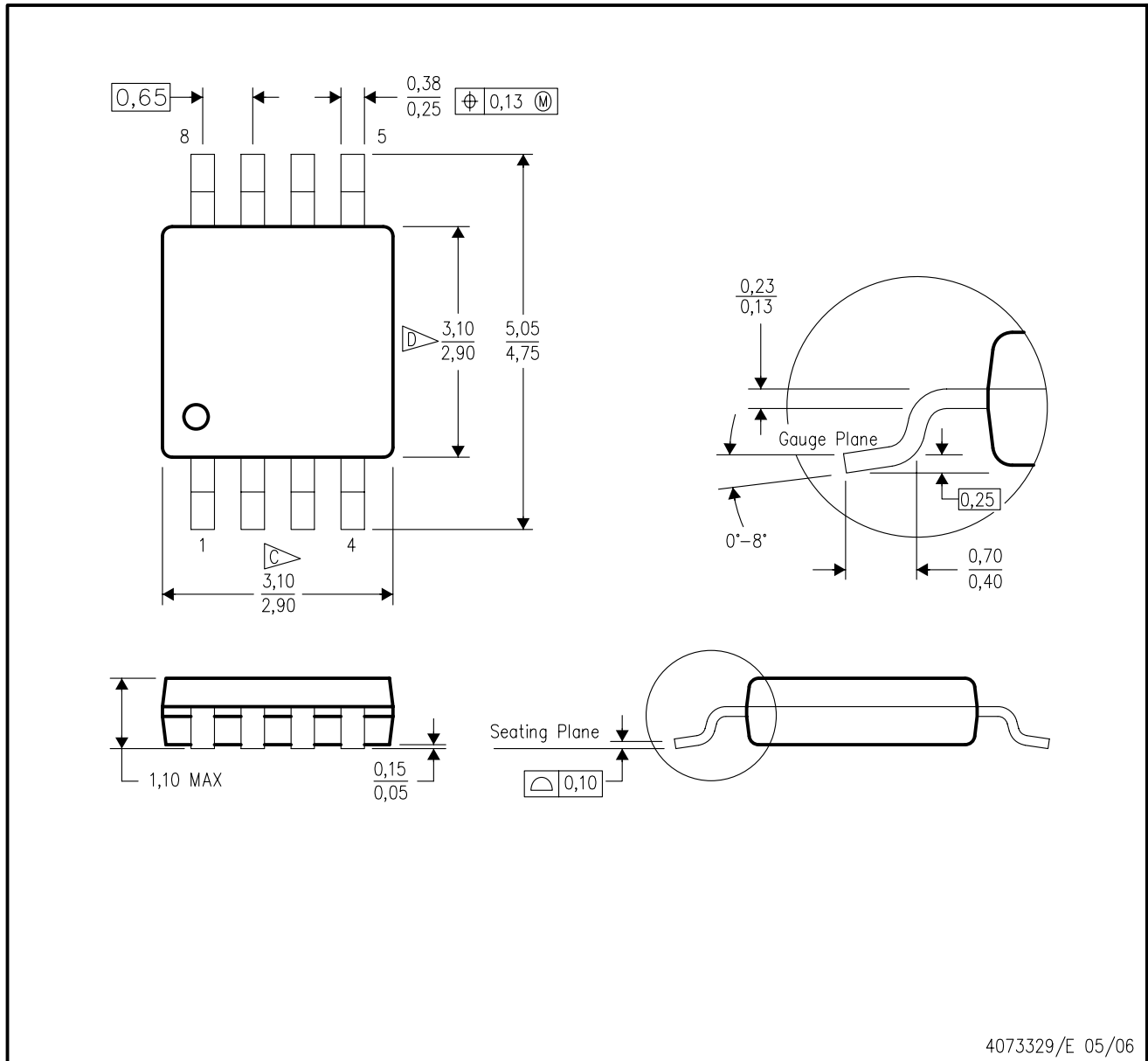
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8501E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
DAC8501E/2K5	VSSOP	DGK	8	2500	853.0	449.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

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 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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