

# OPTIREG™ linear voltage regulator TLS105B0MB

## High-precision voltage tracker



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Technical documents



Simulation



Family overview



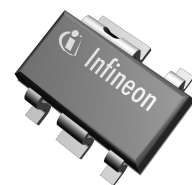
Support



RoHS

## Features

- 50 mA current capability
- Very high tracking accuracy
- Output voltage adjustable down to 2.0 V
- Stable with ceramic output capacitors
- Very low dropout voltage of typically 250 mV at 50 mA
- Very low current consumption of typically 3  $\mu$ A in standby mode
- Wide input voltage range  $-16\text{ V} \leq V_{IN} \leq 45\text{ V}$
- Wide temperature range:  $-40^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$
- Short circuit protected output (to GND and to battery)
- Reverse polarity protected input
- Overtemperature protection
- Green Product (RoHS compliant)



## Potential applications

- Automotive sensor supply
- Protected sensor supply for off-board sensors
- Secondary voltage supply for automotive ECU
- High precision voltage tracking
- Precision voltage replication
- Power switch for off-board load

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

## Description

The OPTIREG™ linear voltage regulator TLS105B0MB is a monolithic, integrated low-dropout voltage tracking regulator with high accuracy in small PG-SCT595-5 package. The TLS105B0MB is designed to supply off-board systems, for example sensors in powertrain management systems under the severe conditions of automotive applications. The TLS105B0MB provides protection functions against reverse polarity as well as against short circuit to GND and to battery. The output voltage follows the reference voltage applied to the EN/ADJ input with very high accuracy, up to a supply voltage of 40 V and up to an output current of 50 mA. The required minimum reference voltage at EN/ADJ is 2.0 V.

**OPTIREG™ linear voltage regulator TLS105B0MB**  
**High-precision voltage tracker**

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**Description**

<b>Type</b>	<b>Package</b>	<b>Marking</b>
TLS105B0MB	PG-SCT595-5	05

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1 Block diagram

1 Block diagram

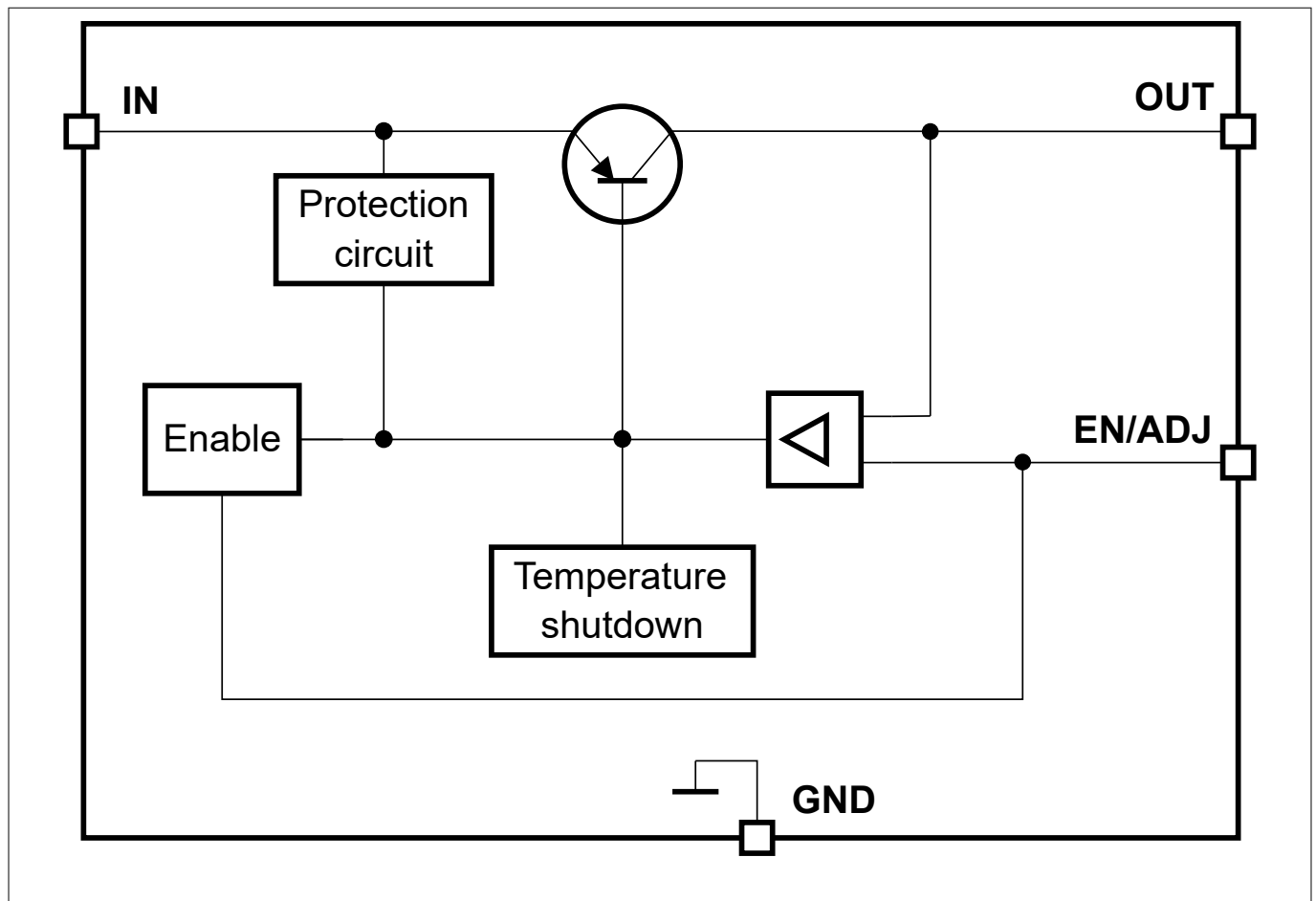
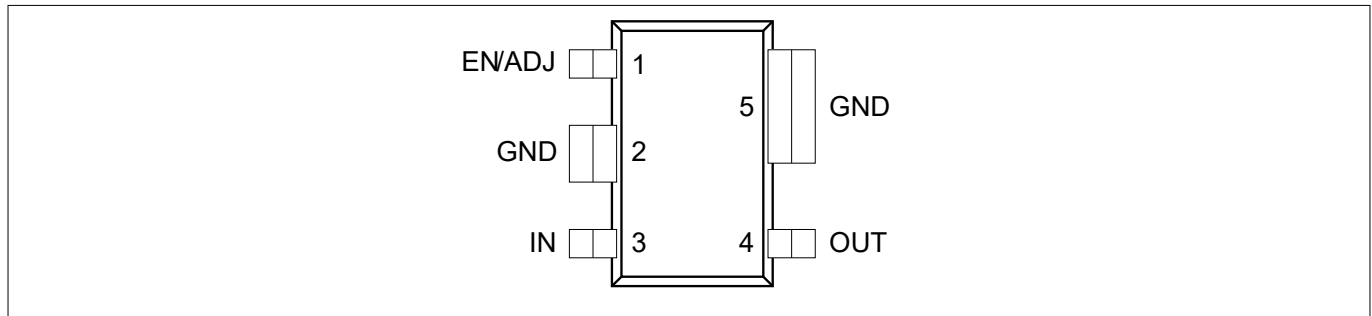


Figure 1 Block diagram

**2 Pin configuration**

**2 Pin configuration**

**2.1 Pin assignment**



**Figure 2 Pin configuration**

**2.2 Pin definitions and functions**

**Table 1 Pin definitions and functions**

Pin	Symbol	Function
1	EN/ADJ	Enable/adjust: Connect the reference voltage to this pin. The reference voltage can be connected directly or via a voltage divider for lower output voltages. For the compensation of disturbances on the line, a capacitor close to the IC pins is recommended. "low" signal disables the device "high" signal enables the device
2	GND	Ground: Internally connected to pin 5. Connect to heatsink area.
3	IN	Input: Compensating line disturbances with a small ceramic capacitor to GND close to the IC terminals is recommended.
4	OUT	Tracker output: 50 mA output current capability Connect a capacitor to GND close to the pin, in accordance with capacitance and ESR requirements described in <a href="#">Table 3</a> .
5	GND	Ground: Internally connected to pin 2. Connect to heatsink area.

**3 General product characteristics**

**3 General product characteristics**

**3.1 Absolute maximum ratings**

**Table 2 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin  
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Voltages</b>							
Input voltage	$V_{IN}$	-16	-	45	V	-	P_3.1.1
Enable/Adjust voltage	$V_{EN/ADJ}$	-0.3	-	45	V	-	P_3.1.2
Output voltage	$V_{OUT}$	-5	-	45	V	-	P_3.1.3
Input output voltage difference	$V_{IN}-V_{OUT}$	-30	-	45	V	-	P_3.1.4
<b>Temperatures</b>							
Junction temperature	$T_j$	-40	-	150	°C	-	P_3.1.5
Storage temperature	$T_{stg}$	-55	-	150	°C	-	P_3.1.6
<b>ESD susceptibility</b>							
ESD susceptibility	$V_{ESD,HBM}$	-2	-	2	kV	<sup>2)</sup> Human Body Model (HBM)	P_3.1.7
ESD susceptibility	$V_{ESD,CDM}$	-1	-	1	kV	<sup>3)</sup> CDM	P_3.1.8
ESD susceptibility	$V_{ESD,CDM}$	-1	-	1	kV	<sup>3)</sup> Charged Device Model (CDM) at corner pins	P_3.1.9

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k  $\Omega$ , 100 pF)

3) Charged device model (CDM) robustness according to ESDA STM5.3.1 or ANSI/ESD S.5.3.1.

**Notes:**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside the normal operating range. Protection functions are not designed for continuous repetitive operation.

**3 General product characteristics**

**3.2 Functional range**

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Input voltage range	$V_{IN}$	4	–	40	V	–	P_3.2.1
Adjust input voltage range (Voltage tracking range)	$V_{ADJ}$	2	–	20	V	–	P_3.2.2
Capacitance of output capacitor	$C_{OUT}$	1	–	–	$\mu\text{F}$	<sup>1)</sup>	P_3.2.3
Equivalent series resistance of output capacitor	$ESR_{C_{OUT}}$	–	–	3	$\Omega$	<sup>2)</sup>	P_3.2.4
Junction temperature	$T_j$	-40	–	150	$^{\circ}\text{C}$	–	P_3.2.5

- 1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%  
2) Relevant ESR value at  $f = 10$  kHz.

*Note:* Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

**3.3 Thermal resistance**

**Table 4 Thermal resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Junction to ambient	$R_{thJA}$	–	84	–	K/W	<sup>2)</sup>	P_3.3.1
Junction to ambient	$R_{thJA}$	–	228	–	K/W	<sup>3)</sup> Footprint only	P_3.3.2
Junction to ambient	$R_{thJA}$	–	123	–	K/W	<sup>3)</sup> 300 mm <sup>2</sup> PCB heatsink area	P_3.3.3
Junction to ambient	$R_{thJA}$	–	109	–	K/W	<sup>3)</sup> 600 mm <sup>2</sup> PCB heatsink area	P_3.3.4
Junction to soldering point	$R_{thJSP}$	–	32	–	K/W	Pins 2, 5 fixed to $T_A$	P_3.3.5

- 1) Not subject to production test, specified by design.  
2) Specified  $R_{thJA}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a  $76.2 \times 114.3 \times 1.5$  mm<sup>3</sup> board with two inner copper layers ( $2 \times 70$   $\mu\text{m}$  Cu,  $2 \times 35$   $\mu\text{m}$  Cu). Where applicable, a thermal via array next to the package contacted the first inner copper layer.  
3) Package mounted on PCB FR4;  $80 \times 80 \times 1.5$  mm<sup>3</sup>; 35  $\mu\text{m}$  Cu, 5  $\mu\text{m}$  Sn; horizontal position; zero airflow.

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit [www.jedec.org](http://www.jedec.org).

## **4 Block description and electrical characteristics**

### **4.1 Functional description tracking regulator**

The regulator controls the output voltage  $V_{OUT}$  by comparing it to the reference voltage applied to the EN/ADJ pin and driving a PNP pass transistor accordingly. The stability of the control loop depends on the following parameters:

- output capacitor  $C_{OUT}$
- load current
- IC temperature
- poles and zeroes in the frequency response of the circuit including TLS105B0MB
- external circuitry

An input capacitor  $C_{IN}$  is strongly recommended to buffer disturbances on the line.

To ensure stable operation, the output capacitor's capacitance and its equivalent series resistance *ESR* must fulfill the requirements in [Table 3](#). The output capacitor must be sized suitably to buffer load transients.

Connect each capacitor close to the pins.

The internal protection features are designed to protect the device itself as well as the application from destruction in case of catastrophic events. These safeguards contain the following:

- Output current limitation
- Reverse polarity protection
- Thermal shutdown

#### **Output current limitation**

In order to protect the pass element and the package from excessive power dissipation, the device limits the maximum output current at high input voltage.

#### **Reverse polarity protection**

The device allows a negative supply voltage. However, in reverse polarity condition several small currents flowing into the device increase the junction temperature. Thermal design must consider this effect, because in reverse polarity condition the overtemperature protection circuit does not operate.

#### **Thermal shutdown**

The overtemperature protection circuit is designed to prevent immediate destruction of the device in certain fault conditions (for example a permanent short circuit at output) by switching off the power stage. After the chip cools down, the regulator restarts. If the fault is not removed, then this leads to an oscillatory behavior of the output voltage. A junction temperature above 150°C is outside the maximum ratings and reduces the lifetime of the device.



**4 Block description and electrical characteristics**

**4.2 Electrical characteristics tracking regulator**

**Table 5 Electrical characteristics tracking regulator**

$V_{IN} = 13.5\text{ V}$ ,  $2.0\text{ V} \leq V_{EN/ADJ} \leq 20\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
<b>Tracking output</b>							
Output voltage tracking accuracy	$\Delta V_{OUT}$	-5	-	5	mV	$\Delta V_{OUT} = V_{ADJ} - V_{OUT}$ ; $4\text{ V} \leq V_{IN} \leq 22\text{ V}$ ; $0.1\text{ mA} \leq I_{OUT} \leq 50\text{ mA}$ ; $2\text{ V} \leq V_{EN/ADJ} \leq V_{IN} - 0.5\text{ V}$ ; $V_{EN/ADJ} \leq 20\text{ V}$	P_4.1.1
Output voltage tracking accuracy	$\Delta V_{OUT}$	-5	-	5	mV	$\Delta V_{OUT} = V_{ADJ} - V_{OUT}$ ; $4\text{ V} \leq V_{IN} \leq 32\text{ V}$ ; $0.1\text{ mA} \leq I_{OUT} \leq 25\text{ mA}$ ; $2\text{ V} \leq V_{EN/ADJ} \leq V_{IN} - 0.5\text{ V}$ ; $V_{EN/ADJ} \leq 20\text{ V}$	P_4.1.2
Output voltage tracking accuracy	$\Delta V_{OUT}$	-5	-	5	mV	$\Delta V_{OUT} = V_{ADJ} - V_{OUT}$ ; $4\text{ V} \leq V_{IN} \leq 40\text{ V}$ ; $0.1\text{ mA} \leq I_{OUT} \leq 10\text{ mA}$ ; $2\text{ V} \leq V_{EN/ADJ} \leq V_{IN} - 0.5\text{ V}$ ; $V_{EN/ADJ} \leq 20\text{ V}$	P_4.1.3
Load regulation steady state	$\Delta V_{OUT,load}$	-3	-	-	mV	$I_{OUT} = 0.1\text{ mA}$ to $50\text{ mA}$ ; $V_{EN/ADJ} = 5\text{ V}$	P_4.1.4
Line regulation steady state	$\Delta V_{OUT,line}$	-	-	3	mV	$V_{IN} = 5.5\text{ V}$ to $32\text{ V}$ ; $I_{OUT} = 10\text{ mA}$ ; $V_{EN/ADJ} = 5\text{ V}$	P_4.1.5
Power supply ripple rejection	$PSRR$	-	100	-	dB	<sup>1)</sup> $f_{ripple} = 100\text{ Hz}$ ; $V_{ripple} = 1\text{ V}_{pp}$ ; $I_{OUT} = 10\text{ mA}$ ; $C_{OUT} = 10\text{ }\mu\text{F}$ , ceramic type	P_4.1.6
Output current limitation	$I_{OUT,max}$	51	85	120	mA	$V_{OUT} = V_{ADJ} - 0.1\text{ V}$ ; $V_{EN/ADJ} = 5\text{ V}$	P_4.1.7
Reverse current	$I_{OUT,rev}$	-1	-0.3	-	mA	$V_{IN} = 0\text{ V}$ ; $V_{OUT} = 16\text{ V}$ ; $V_{EN/ADJ} = 5\text{ V}$	P_4.1.10
Reverse current at negative input voltage	$I_{IN,rev}$	-8	-4	-	mA	$V_{IN} = -16\text{ V}$ ; $V_{OUT} = 0\text{ V}$ ; $V_{EN/ADJ} = 5\text{ V}$	P_4.1.11

**(table continues...)**

**4 Block description and electrical characteristics**

**Table 5 (continued) Electrical characteristics tracking regulator**

$V_{IN} = 13.5\text{ V}$ ,  $2.0\text{ V} \leq V_{EN/ADJ} \leq 20\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Dropout voltage	$V_{dr}$	–	250	450	mV	<sup>2)</sup> $V_{dr} = V_{IN} - V_{OUT}$ ; $I_{OUT} = 50\text{ mA}$ ; $V_{EN/ADJ} = 5\text{ V}$	P_4.1.12
<b>Overtemperature protection<sup>1)</sup></b>							
Overtemperature shutdown threshold	$T_{j,sd}$	–	175	–	°C	$T_j$ increasing due to power dissipation generated by the device	P_4.1.16
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	°C		P_4.1.17

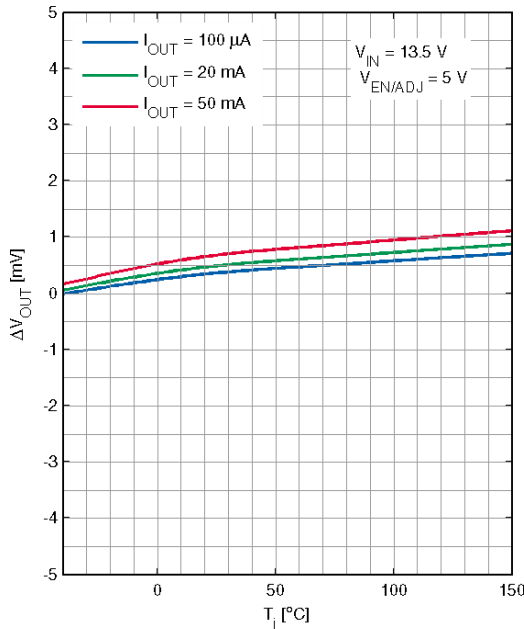
1) Not subject to production test, specified by design.

2) Measured when the output voltage  $V_O$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5\text{ V}$ .

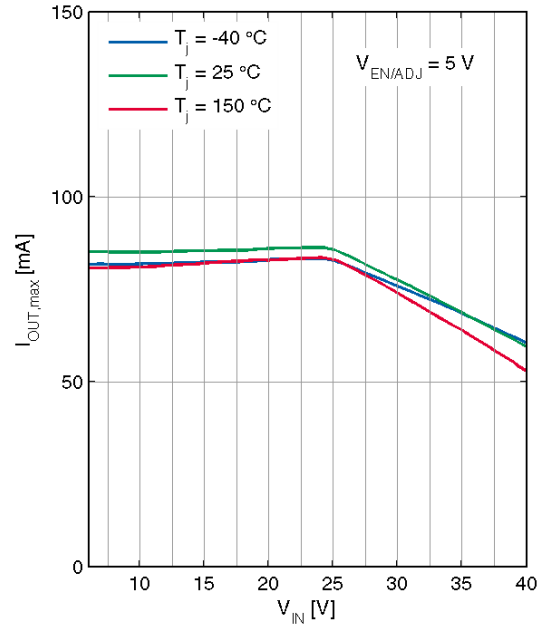
**4 Block description and electrical characteristics**

**4.3 Typical performance characteristics tracking regulator**

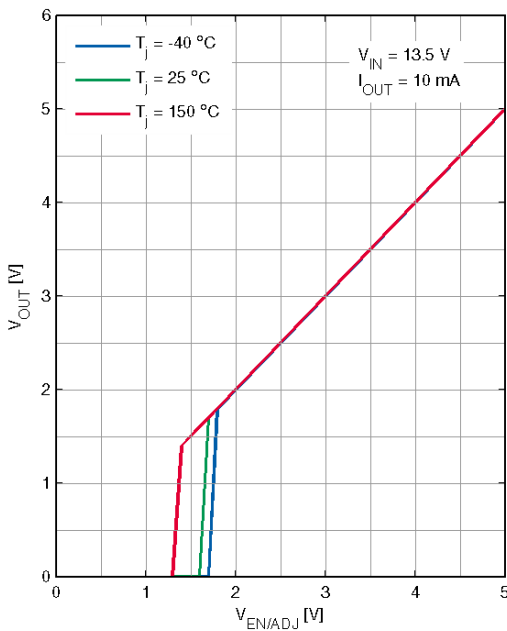
Tracking accuracy  $\Delta V_{OUT}$  versus junction temperature  $T_j$



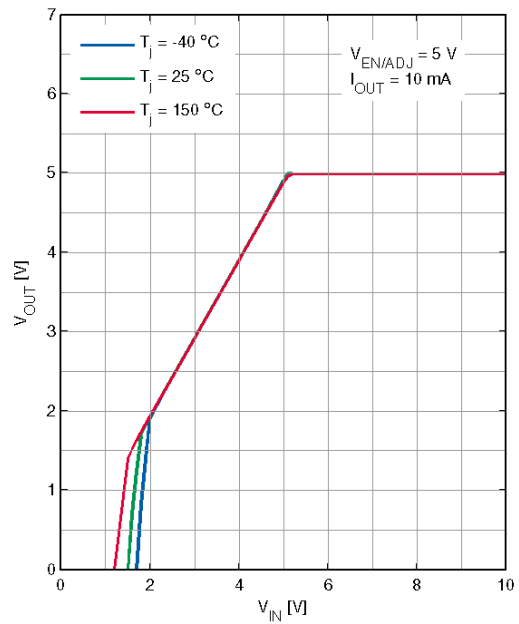
Output current limitation  $I_{OUT,max}$  versus input voltage  $V_{IN}$



Output voltage  $V_{OUT}$  versus enable/adjust voltage  $V_{EN/ADJ}$

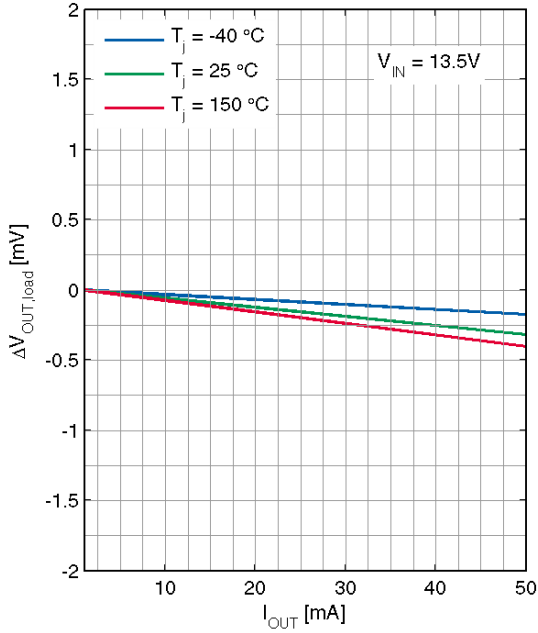


Output voltage  $V_{OUT}$  versus input voltage  $V_{IN}$

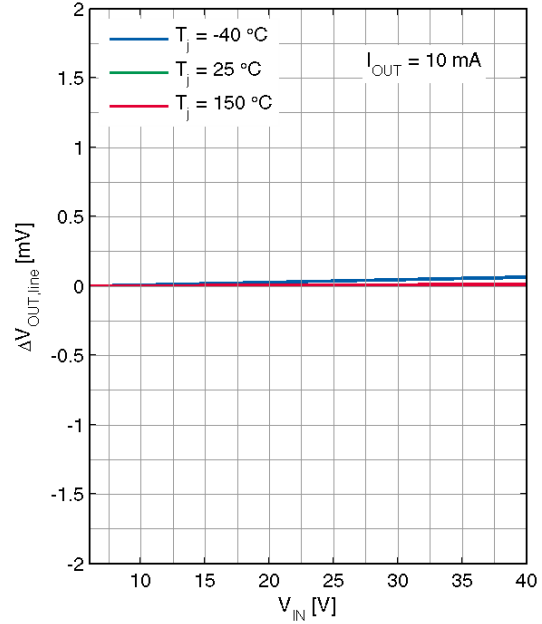


**4 Block description and electrical characteristics**

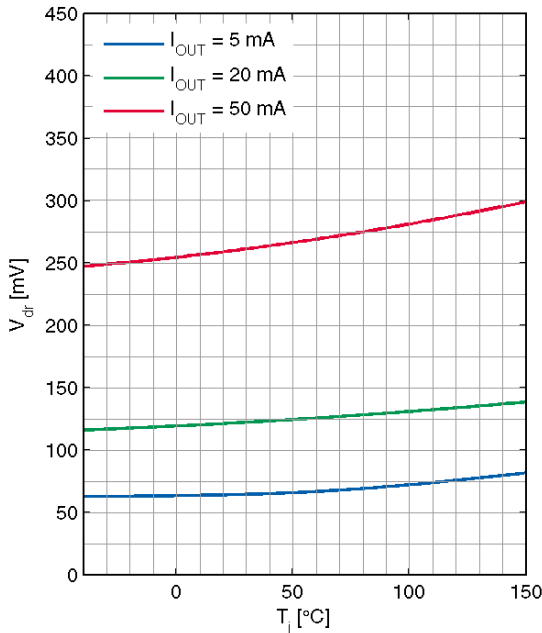
Load regulation  $\Delta V_{OUT,load}$  versus output current  $I_{OUT}$



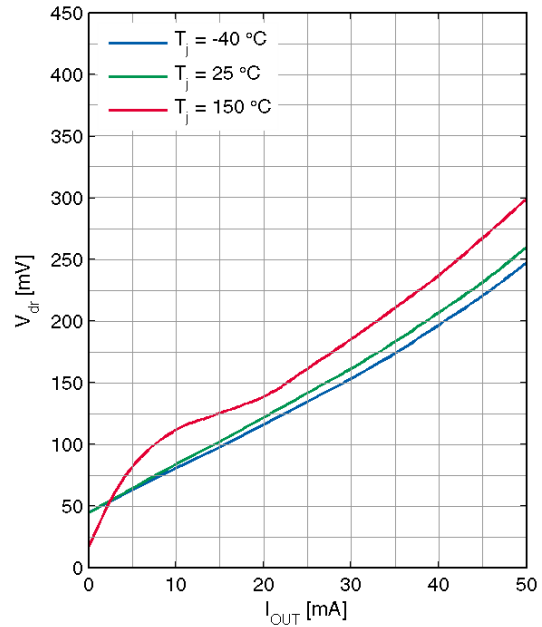
Line regulation  $\Delta V_{OUT,line}$  versus input voltage  $V_{IN}$



Dropout voltage  $V_{dr}$  versus junction temperature  $T_j$

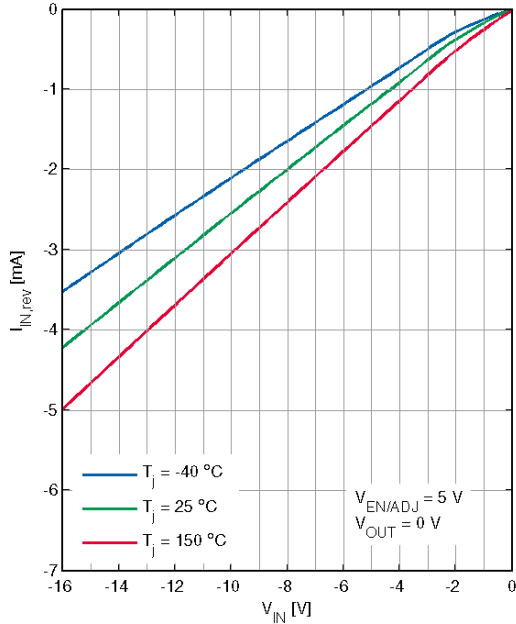


Dropout voltage  $V_{dr}$  versus output current  $I_{OUT}$

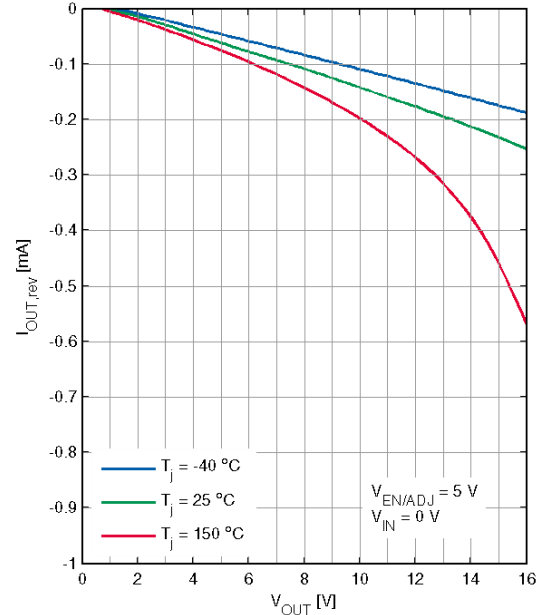


**4 Block description and electrical characteristics**

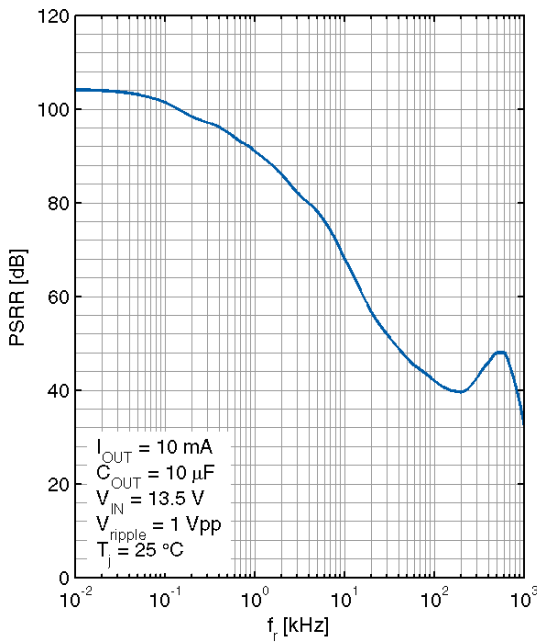
Reverse input current  $I_{IN,rev}$  versus input voltage  $V_{IN}$



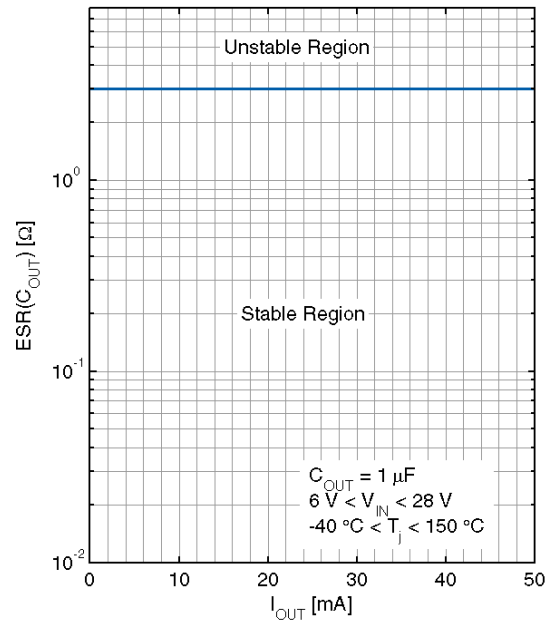
Reverse output current  $I_{OUT,rev}$  versus output voltage  $V_{OUT}$



Power supply ripple rejection  $PSRR$  versus ripple frequency  $f_r$



Output capacitor equivalent series resistance  $ESR_{C_{OUT}}$  versus output current  $I_{OUT}$



**4 Block description and electrical characteristics**

**4.4 Electrical characteristics current consumption**

**Table 6 Electrical characteristics current consumption**

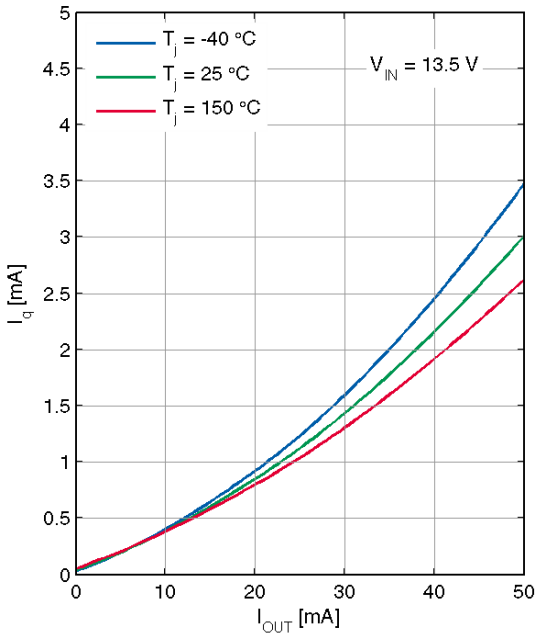
$V_{IN} = 13.5\text{ V}$ ,  $2.0\text{ V} \leq V_{EN/ADJ} \leq 20\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption stand-by mode	$I_{q,off}$	–	3	4.5	$\mu\text{A}$	$I_{q,off} = I_{IN}$ ; $V_{EN/ADJ} \leq 0.4\text{ V}$ ; $T_j \leq 125^\circ\text{C}$
Current consumption	$I_q$	–	40	75	$\mu\text{A}$	$I_q = I_{IN} - I_{OUT}$ ; $I_{OUT} \leq 0.1\text{ mA}$ ; $V_{EN/ADJ} = 5\text{ V}$ ; $T_j \leq 125^\circ\text{C}$
Current consumption	$I_q$	–	3	5.5	$\text{mA}$	$I_q = I_{IN} - I_{OUT}$ ; $I_{OUT} \leq 50\text{ mA}$ ; $V_{EN/ADJ} = 5\text{ V}$

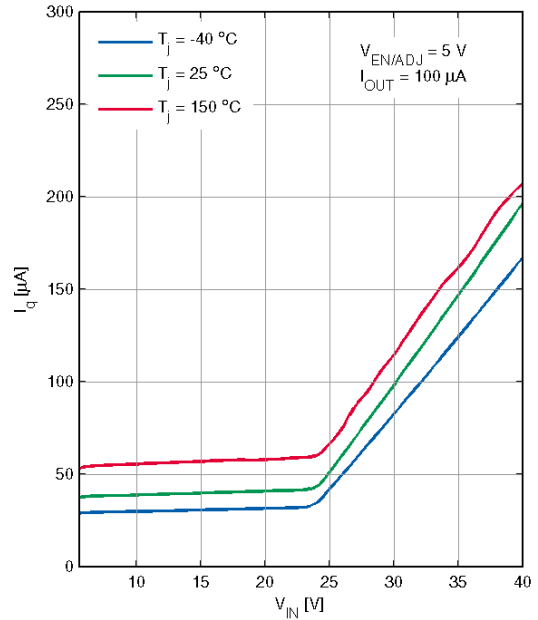
**4 Block description and electrical characteristics**

**4.5 Typical performance characteristics current consumption**

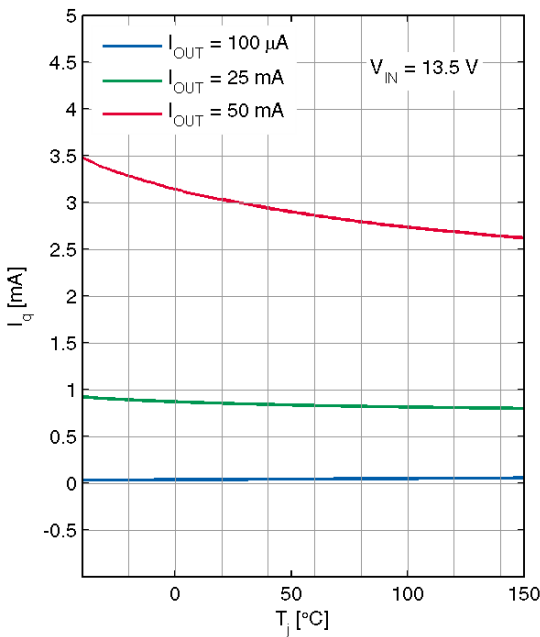
Current consumption  $I_q$  versus output current  $I_{OUT}$



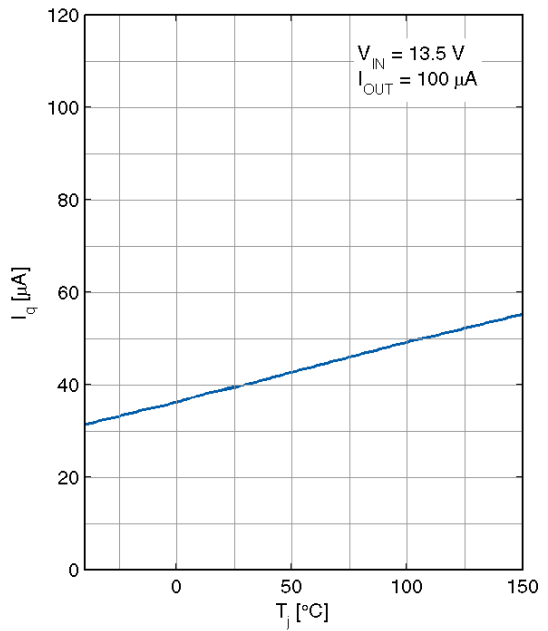
Current consumption  $I_q$  versus input voltage  $V_{IN}$



Current consumption  $I_q$  versus junction temperature  $T_j$

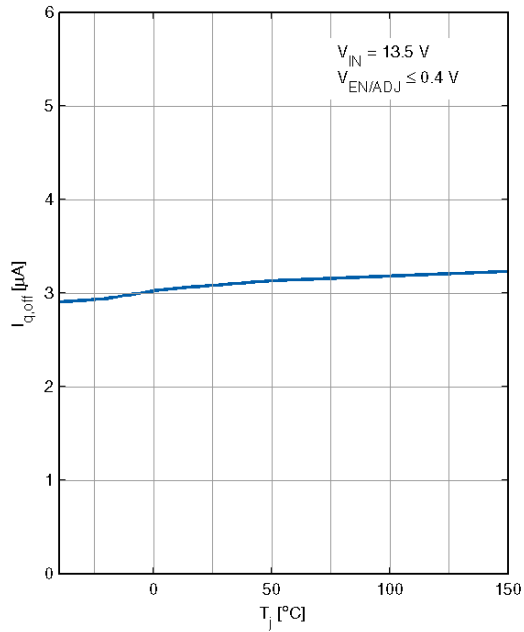


Current consumption  $I_q$  versus junction temperature  $T_j$  ( $I_{OUT}$  low)



**4 Block description and electrical characteristics**

Current consumption in OFF mode  $I_{q,off}$  versus junction temperature  $T_j$





## 4 Block description and electrical characteristics

### 4.6 Functional description enable/adjust input

On a “low” signal at the enable/adjust input EN/ADJ the device switches to standby mode in order to minimize the quiescent current.

If the EN/ADJ pin is not connected, then the “low” level from the internal pull-down resistor switches off the regulator.

### 4.7 Electrical characteristics enable/adjust input

**Table 7 Electrical characteristics enable/adjust input**

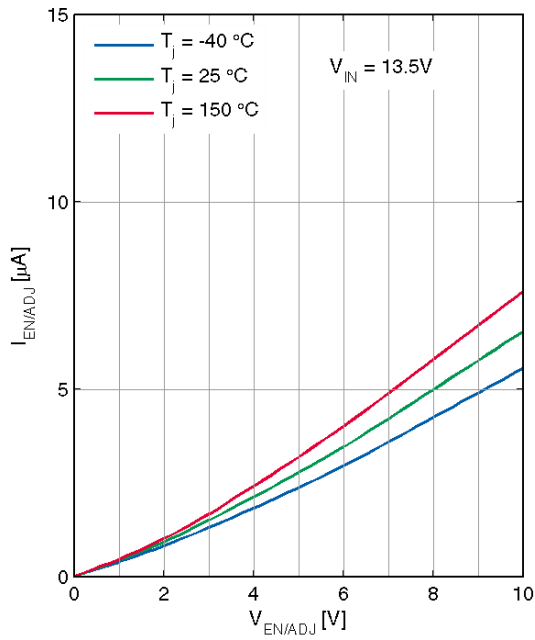
$V_{IN} = 13.5\text{ V}$ ,  $2.0\text{ V} \leq V_{EN/ADJ} \leq 20\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Enable/adjust off voltage range	$V_{EN/ADJ,off}$	–	–	0.8	V	$V_{OUT} = 0\text{ V}$
Enable/adjust on voltage range	$V_{EN/ADJ,on}$	2	–	–	V	$V_{OUT}$ settled
Enable/adjust input current	$I_{EN/ADJ}$	–	3	5	$\mu\text{A}$	$V_{EN/ADJ} = 5\text{ V}$

**4 Block description and electrical characteristics**

**4.8 Typical performance characteristics enable/adjust input**

Enable/adjust input current  $I_{EN/ADJ}$  versus  
input voltage  $V_{EN/ADJ}$

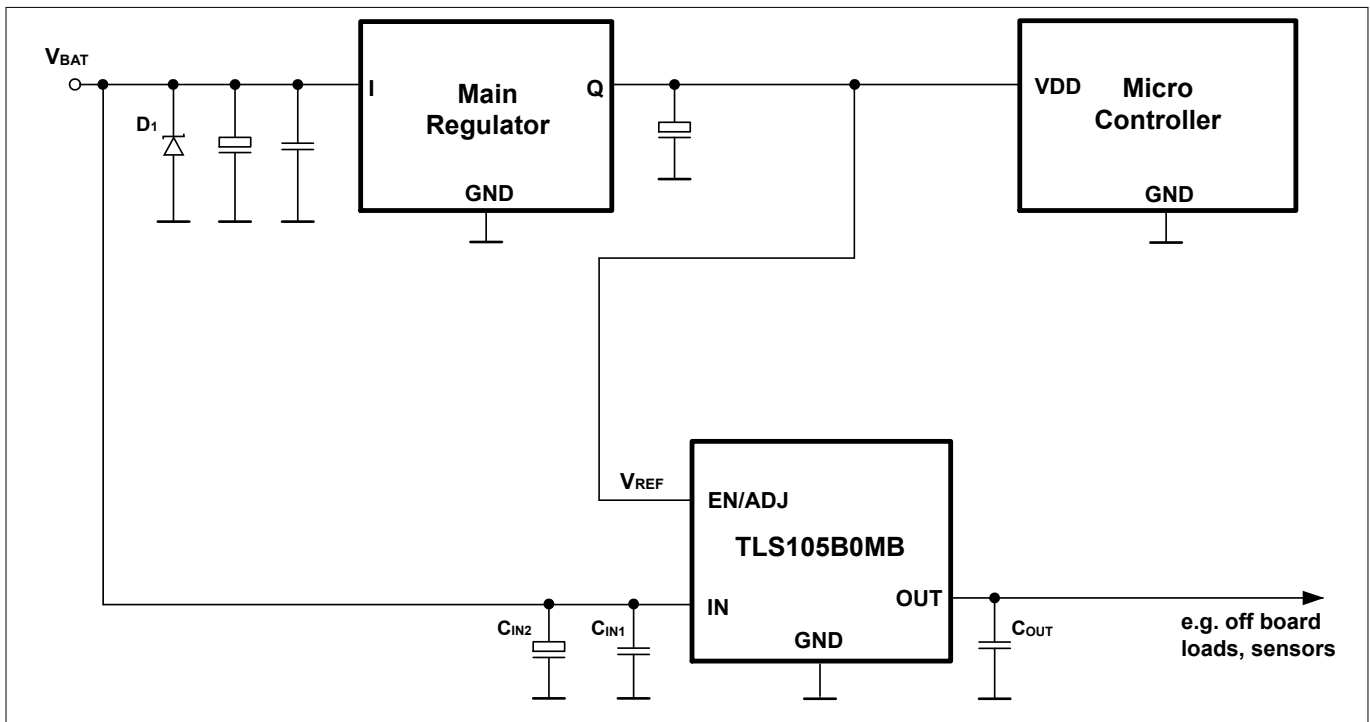


**5 Application information**

**5 Application information**

*Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

**5.1 Application diagram**



**Figure 3 Application circuit**

*Note: This figure is a simplified example of an application circuit. The function must be verified in the application.*

**5.2 Selection of external components**

**5.2.1 Input pin**

Figure 3 shows a typical input circuitry for a voltage tracking regulator. The following external components at the input are recommended in case of possible external disturbance.

**Ceramic capacitor**

A ceramic capacitor  $C_{IN1}$  (100 nF to 470 nF) at the input filters high frequency disturbance imposed by the line, such as ISO pulses 3a/b. Place  $C_{IN1}$  as close as possible to the input pin of the voltage tracking regulator on the PCB.

**Aluminum electrolytic capacitor**

An aluminum electrolytic capacitor  $C_{IN2}$  (10  $\mu$ F to 470  $\mu$ F) at the input smoothens high energy pulses, such as ISO pulse 2a. Place  $C_{IN2}$  close to the input pin of the voltage tracking regulator on the PCB.

## 5 Application information

### Overvoltage suppression diode

A suitably sized diode  $D_1$  suppresses high voltage beyond the maximum ratings of the circuit components and protects the device from damage due to overvoltage.

### 5.2.2 Output pin

An output capacitor  $C_{OUT}$  is necessary for the stability of the voltage tracking regulator, see [Table 3](#). The typical performance graph [Output capacitor equivalent series resistance ESR<sub>COUT</sub> versus output current I<sub>OUT</sub>](#) shows the stable operating range of the device.

In an automotive environment, ceramic capacitors with X5R or X7R dielectrics are recommended.

Place  $C_{OUT}$  on the same side of the PCB as the device and as close as possible to both the OUT pin and the GND pin.

In case of rapid transients of the input voltage or of the load current,  $C_{OUT}$  must be dimensioned properly to ensure the output stability in the application.

### 5.2.3 Enable/Adjust pin

[Figure 3](#) shows the typical input circuitry for a voltage tracking regulator. Typically the enable/adjust pin is connected to a fixed voltage reference that the regulator tracks. In the example of the application diagram EN/ADJ is connected to the supply voltage of a microcontroller. Alternatively, the voltage reference can also be adjusted by a voltage divider.

## 5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_q$$

### Equation 1

with

- $P_D$ : continuous power dissipation
- $V_{IN}$ : input voltage
- $V_{OUT}$ : output voltage
- $I_{OUT}$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated by:

$$R_{thJA, max} = \frac{T_{j, max} - T_a}{P_D}$$

### Equation 2

with

- $T_{j, max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

## 5 Application information

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in [Table 4](#).

### Example

Application conditions:

- $V_{IN} = 13.5 \text{ V}$
- $V_{OUT} = V_{ADJ} = 5 \text{ V}$
- $I_{OUT} = 20 \text{ mA}$
- $T_a = 125^\circ\text{C}$

Calculation of  $R_{thJA,max}$ :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_q = (13.5 \text{ V} - 5 \text{ V}) \times 20 \text{ mA} + 13.5 \text{ V} \times 0.9 \text{ mA} = 0.182 \text{ W}$$

### Equation 3

$$R_{thJA,max} = \frac{T_{j,max} - T_a}{P_D} = \frac{150^\circ\text{C} - 125^\circ\text{C}}{0.182 \text{ W}} = 137 \text{ K/W}$$

### Equation 4

As a result, the PCB design must ensure a thermal resistance  $R_{thJA,max}$  lower than 137 K/W.

According to [Table 4](#), at least 300 mm<sup>2</sup> heatsink area is required on the FR4 1s0p PCB, or the FR4 2s2p board can be used.



**Revision history**

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## Revision history

Revision	Date	Changes
1.13	2022-11-10	Editorial changes
1.12	2021-05-28	Editorial changes
1.11	2020-10-12	Editorial changes
1.1	2018-07-31	Datasheet updated: <ul style="list-style-type: none"><li>• Package outline drawing:<ul style="list-style-type: none"><li>- algebraic sign "+" → "-" for some tolerance values</li><li>- add pin 1 to pin 3 distance</li></ul></li><li>• Editorial changes</li></ul>
1.0	2018-01-22	Datasheet created

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