PCN Number:	20170418000	PCN Date:	April 24, 2017
Title:	Datasheet for ADC3441, ADC3442, ADC3443, ADC3444		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

ADC3441, ADC3442, ADC3443, ADC3444

SBAS670B – JULY 2014 – REVISED APRIL 2017

Changes from Revision A (October 2015) to Revision B **Page**

- Added description for availability of one-wire serial LVDS interface in *Description* section ... 1
- Changed *Spectrum at 10 MHz* figure to show conditions within curve ... 1
- Changed description of AVDD, DVDD, and GND pins and added *active high* to description of PDN pin in *Pin Functions* table ... 5
- Deleted *maximum* from parameter description in *Recommended Operating Conditions* table ... 6
- Changed Digital Outputs, R_{LOAD} parameter description in *Recommended Operating Conditions* table ... 6
- Changed conditions of all *Electrical Characteristics* and *AC Performance* tables ... 7
- Added minimum and maximum specifications to Analog Input, $V_{OC(VCM)}$ parameter in *Electrical Characteristics: General* table ... 7
- Changed description of Analog Input, *Analog input bandwidth* parameter in *Electrical Characteristics: General* table ... 7
- Deleted footnote 1 from *Electrical Characteristics: General* table ... 7
- Added DC Accuracy, E_G parameter with its test conditions and footnote 3 to *Electrical Characteristics: General* table ... 7
- Deleted $E_{G(REF)}$ and $E_{G(CHAN)}$ from DC Accuracy in *Electrical Characteristics: General* table ... 7
- Changed DC Accuracy, $\alpha_{(EGCHAN)}$ to α_{EG} and updated its parameter in *Electrical Characteristics: General* table ... 7
- Changed Channel-to-Channel Isolation, *Crosstalk* parameter in *Electrical Characteristics: General* table: changed test conditions, added footnote 2 ... 7
- Changed test conditions for IMD3 parameter in *AC Performance: ADC3441* table ... 10
- Added INL and DNL rows to all *AC Performance* tables ... 10
- Changed *Digital Inputs (SYSREFP, SYSREFM)* subsection in *Digital Characteristics* table, added footnote 2 ... 17

- Changed specifications of Digital Outputs (LVDS Interface), V_{OCM} parameter in *Digital Characteristics* table 17
- Changed *rising* to *falling* in description of *SYSREF reference time* parameter in *Timing Requirements: General* table 17
- Changed *Typical Characteristics* sections: added *dither on* to all section condition statements, changed *Non 23* to *excluding HD2, HD3* 19
- Added INL and DNL plots in Typical Characteristics: ADC3441 section 24
- Changed conditions of Figure 34, Figure 35 25
- Added INL and DNL plots in Typical Characteristics: ADC3442 section 30
- Changed conditions of Figure 67, Figure 68 31
- Added INL and DNL plots in Typical Characteristics: ADC3443 section 36
- Changed conditions of Figure 100, Figure 101 37
- Added INL and DNL plots in Typical Characteristics: ADC3444 section. 42
- Changed conditions of Figure 134 43
- Added Figure 141 to *Timing Diagrams* section 44
- Added *Using the SYSREF Input* section 50
- Changed the description about synchronization of the phase of the divided clock in each device to the common sampling clock in Using the SYSREF Input section. 50
- Added *ADC3441 Power-Up Requirements* section, deleted the *Register Initialization* section 57
- Added last sentence to *Detailed Design Procedure* section of first typical application 75
- Added *Chopper On* to caption of Figure 198 75
- Added *Chopper Off* to caption of Figure 200 76
- Changed the caption of Figure 202 from *FFT for 450-MHz Input Signal (Dither On)* to *FFT for 450-MHz Input Signal (Chopper Off, Dither On)* 77

The datasheet number will be changing.

Device Family	Change From:	Change To:
ADC3441, ADC3442, ADC3443, ADC3444	SBAS670A	SBAS670B

These changes may be reviewed at the datasheet links provided.
http://www.ti.com/product/ADC3441

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

ADC3441IRTQR	ADC3441IRTQT	ADC3442IRTQR	ADC3442IRTQT
ADC3443IRTQR	ADC3443IRTQT	ADC3444IRTQR	ADC3444IRTQT

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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