PIC16C76/77 → PIC16F76/77 Migration

DEVICE MIGRATIONS

This document is intended to describe the differences that are present when migrating from one device to the next. Table 1 and Table 2 list the data memory organization differences and the additional Special Function Registers, Table 3 lists the differences in functionality, and Table 4 through Table 11 list the differences in the electrical and timing specifications.

Note 1: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

2: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

XT Oscillator Differences

Please refer to the PIC16F73/74/76/77 Rev. B1 Silicon Errata for more information. Please refer to the difference in parameter D042A in Table 5.

$\overline{\text{MCLR}}$ Functionality Differences

The behavior of the ESD protection on the $\overline{\text{MCLR}}$ pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both $\overline{\text{MCLR}}$ Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the $\overline{\text{MCLR}}$ pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 1, is suggested.

FIGURE 1: RECOMMENDED $\overline{\text{MCLR}}$ CIRCUIT

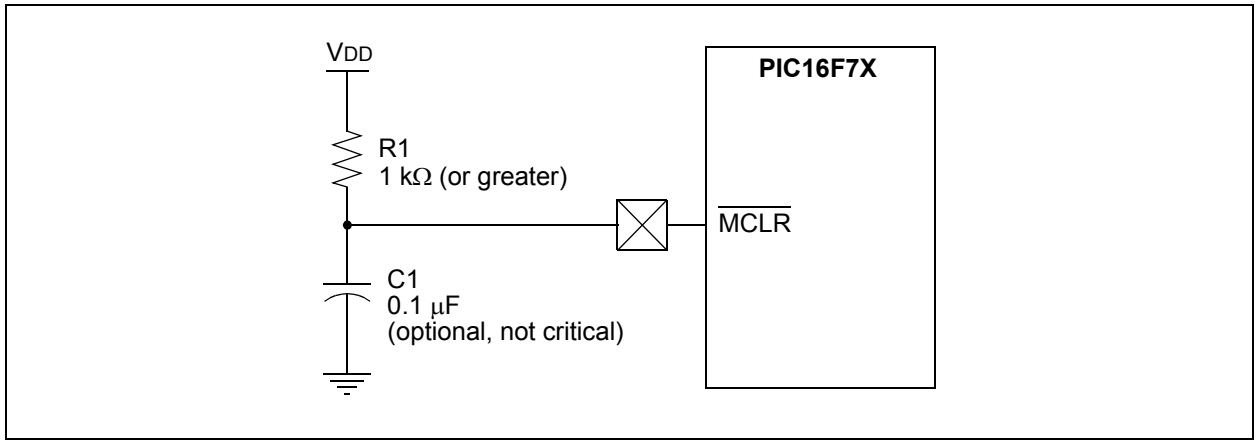

TABLE 1: PIC16C76/77 → PIC16F76/77 DATA MEMORY DIFFERENCES

No.	SFR	Differences from PIC16C76/77	Comment
1	PMADRH:PMADRL	Implemented	Address register pair
2	PMDATH:PMDATL	Implemented	Data register pair
3	PMCON1	Implemented	Control register for memory access
4	INTCON	Bit 2 (TMR0IF) and Bit 5 (TMR0IE)	T0IF and T0IE in PIC16C76/77

TABLE 2: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS(3)
Bank 2											
100h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
101h	TMR0	Timer0 Module's Register								xxxx xxxx	uuuu uuuu
102h(1	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
103h(1)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
104h(1)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
105h	—	Unimplemented								—	—
106h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
10Bh(1)	INTCON	GIE	PEIE	TMR0IE(5)	INTE	RBIE	TMR0IF(5)	INTF	RBIF	0000 000x	0000 000u
10Ch(5)	PMDATL	Data Register Low Byte								xxxx xxxx	uuuu uuuu
10Dh(5)	PMADRL	Address Register Low Byte								xxxx xxxx	uuuu uuuu
10Eh(5)	PMDATH	—	—	Data Register High Byte						xxxx xxxx	uuuu uuuu
10Fh(5)	PMADRH	—	—	—	Address Register High Byte					xxxx xxxx	uuuu uuuu
Bank 3											
180h(1)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
181h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
182h(1)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
183h(1)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
184h(1)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	uuuu uuuu
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
18Bh(1)	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
18Ch(5)	PMCON1	—(4)	—	—	—	—	—	—	RD	1--- ---0	1--- ---0
18Dh	—	Unimplemented								—	—
18Eh	—	Reserved, maintain clear								0000 0000	0000 0000
18Fh	—	Reserved, maintain clear								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, — = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) RESETS include external RESET through $\overline{MCLR}$ and Watchdog Timer Reset.

4: This bit always reads as a '1'.

5: Difference from PIC16C76/77.

FIGURE 2: PIC16F76/77 BANK 2 & 3 REGISTER FILE MAP

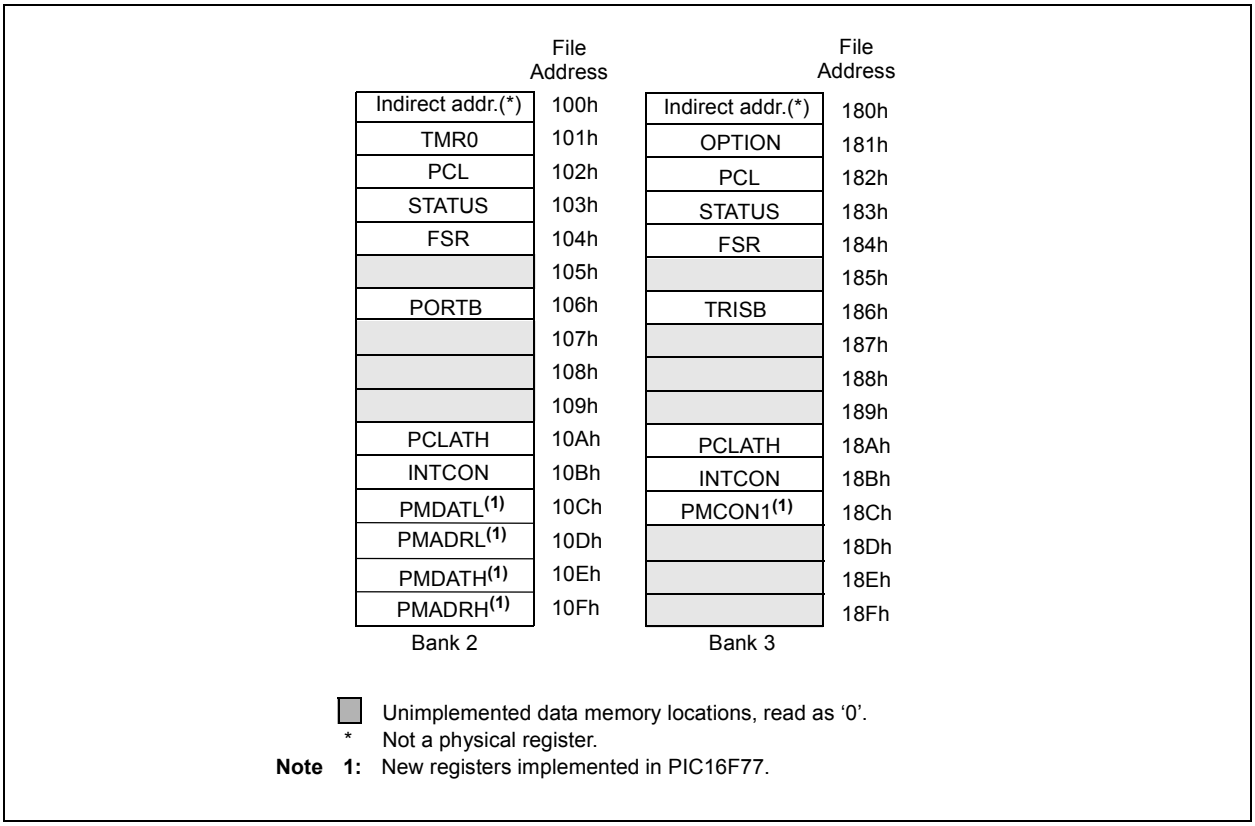

TABLE 3: PIC16C76/77 → PIC16F76/77 FUNCTIONAL DIFFERENCES

No.	Module	Differences from PIC16C76/77	H/W	S/W	Prog
1	Program Memory Read	The FLASH Program Memory is readable during normal operation	—	Yes	—

Legend: H/W - Issues may exist with regard to the application circuit.
S/W - Issues may exist with regard to the user program.
Prog. - Issues may exist with regard to programming.

READING PROGRAM MEMORY

The FLASH Program Memory is readable during normal operation over the entire VDD range. It is indirectly addressed through Special Function Registers (SFR). Up to 14-bit numbers can be stored in memory for use as calibration parameters, serial numbers, packed 7-bit ASCII, etc. Executing a program memory location containing data that forms an invalid instruction results in a NOP.

There are five SFRs used to read the program and memory:

- PMCON1
- PMDATL
- PMDATH
- PMADRL
- PMADRH

The program memory allows word reads. Program memory access allows for checksum calculation and reading calibration tables.

When interfacing to the program memory block, the PMDATH:PMDATL registers form a two-byte word that holds 14-bit data for reads. The PMADRH:PMADRL registers form a two-byte word that holds the 13-bit address of the FLASH location being accessed. This device can have up to 8K words of program FLASH, with an address range from 0h to 1FFFh. The unused upper bits in both the PMDATH and PMADRH registers are not implemented and read as zeroes.

PMADR

The address registers can address up to a maximum of 8K words of program FLASH.

When selecting a program address value, the MSByte of the address is written to the PMADRH register and the LSByte is written to the PMADRL register. The upper MSbits of PMADRH must always be clear.

PMCON1 Register

PMCON1 is the control register for memory access.

The control bit, RD, initiates read operations. This bit cannot be cleared, only set, in software. It is cleared in hardware at the completion of the read operation.

REGISTER 1: PMCON1: PROGRAM MEMORY CONTROL REGISTER (ADDRESS 18Ch)

R-1	U-0	U-0	U-0	U-x	U-0	U-0	R/S-0
reserved	—	—	—	—	—	—	RD
bit 7							bit 0

bit 7 **Reserved:** Read as ‘1’

bit 6-1 **Unimplemented:** Read as ‘0’

bit 0 **RD:** Read Control bit

1 = Initiates a FLASH read, RD is cleared in hardware. The RD bit can only be set (not cleared) in software.

0 = Does not initiate a FLASH read

Legend:		
S = Settable bit	U = Unimplemented bit, read as ‘0’	
W = Writable bit	R = Readable bit	-n = Value at POR
‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 2: CONFIGURATION WORD (ADDRESS 2007h)(1)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	u-1	U-1	u-1	u-1	u-1	u-1	u-1
—	—	—	—	—	—	—	BOREN	—(3)	CP	$\overline{\text{PWRTEN}}$	WDTEN	F0SC1	F0SC0
bit13													bit0

bit 13-7 **Unimplemented:** Read as '1'

bit 6 **BOREN:** Brown-out Reset Enable bit(2)
1 = BOR enabled
0 = BOR disabled

bit 5 **Unimplemented:** Read as '1'

bit 4 **CP:** FLASH Program Memory Code Protection bit
1 = Code protection off
0 = All memory locations code protected

bit 3 **$\overline{\text{PWRTEN}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0:** Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: The erased (unprogrammed) value of the configuration word is 3FFFh.

2: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT), regardless of the value of bit $\overline{\text{PWRTEN}}$. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.

3: Difference from PIC16C76/77.

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
- n = Value when device is unprogrammed		u = Unchanged from programmed state

TABLE 4: PIC16C76/77 → PIC16F76/77 ELECTRICAL CHARACTERISTICS DIFFERENCES

Characteristic	PIC16C7X Data Sheet	PIC16F7X Data Sheet	Units
Voltage on VDD with respect to Vss	-0.3 to 7.5	-0.3 to 6.5	V
Voltage on $\overline{MCLR}$ with respect to Vss (Note 1)	0 to 14	0 to 13.5	V
Voltage on RA4 with respect to Vss	0 to 14	0 to 12	V

Note 1: It is not recommended to tie the $\overline{MCLR}$ pin directly to VDD (see Figure 1 in this document or Figure 12-5 in the PIC16F76/77 Data Sheet for the recommended $\overline{MCLR}$ circuit).

TABLE 5: PIC16C76/77 → PIC16F76/77 DC CHARACTERISTICS DIFFERENCES

Param No.	Sym	Characteristic	PIC16C7X Data Sheet				Conditions	PIC16F7X Data Sheet				Conditions
			Min	Typ†	Max	Units		Min	Typ†	Max	Units	
D001	VDD	**Supply Voltage**	4.0	—	6.0	V	XT, RC and LP osc configuration	4.0	—	5.5	V	All configurations
D001A			4.5	—	5.5	V	HS osc configuration					
D005	BVDD	**Brown-out Reset Voltage**	3.7	4.0	4.3	V	BODEN bit in configuration word enabled	3.65	4.0	4.35	V	Same as PIC16C76/77
D010	IDD	**Supply Current (Notes 3, 5)**	—	2.7	5	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 5.5V, **(Note 5)**	—	0.9	4	mA	XT, RC osc configuration
D013			—	10	20	mA	HS osc configuration FOSC = 20 MHz, VDD = 5.5V	—	5.2	15	mA	HS osc configuration
D015*	ΔIBOR	**Brown-out Reset Current (Note 6)**	—	350	425	μA	BOR enabled, VDD = 5.0V	—	25	200	μA	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: For RC osc configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F76/77 be driven with external clock in RC mode.

2: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
$\overline{OSC1}$ = External square wave, from-rail to-rail; all I/O pins tri-stated, pulled to VDD.
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

4: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

5: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

TABLE 5: PIC16C76/77 → PIC16F76/77 DC CHARACTERISTICS DIFFERENCES (CONTINUED)

Param No.	Sym	Characteristic	PIC16C7X Data Sheet				Conditions	PIC16F7X Data Sheet				Conditions
			Min	Typ†	Max	Units		Min	Typ†	Max	Units	
D020	IPD	**Power-down Reset Current (Note 4, 7)**	—	10.5	42	μA	VDD = 4.0V, WDT enabled, -40°C to +85°C	—	5.0	42	μA	Same as PIC16C76/77
D021x			—	1.5	19	μA	VDD = 4.0V, WDT disabled, -40°C to 85°C	—	0.1	19	μA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B			—	2.5	19	μA	VDD = 4.0V, WDT disabled, -40°C to +125°C	—	1.5	42	μA	Same as PIC16C76/77
D023*	DIBOR	**Brown-out Reset Current (Note 5)**	—	300	425	μA	BOR Enabled, VDD = 5.0V	—	25	200	μA	Same as PIC16C76/77
D042A	VIH	**OSC1 (in XT and LP mode)**	0.7VDD	—	VDD	V		1.6V	—	VDD	V	
D130	EP	**Program FLASH Memory Endurance**	N/A	N/A	N/A	N/A		100	1000	—	E/W	25°C at 5V
D131	VPR	**Program FLASH Memory VDD for Read**	N/A	N/A	N/A	N/A		4.0	—	5.5	V	
D150*	VOD	**Open Drain High Voltage**	—	—	14	V	RA4 pin	—	—	12	V	RA4 pin

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: For RC osc configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F76/77 be driven with external clock in RC mode.

2: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = External square wave, from-rail to-rail; all I/O pins tri-stated, pulled to VDD.
MCLR = VDD; WDT enabled/disabled as specified.

4: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

5: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

TABLE 6: PIC16LC76/77 → PIC16LF76/77 DC CHARACTERISTICS DIFFERENCES

Param No.	Sym	Characteristic	PIC16C7X Data Sheet				Conditions	PIC16F7X Data Sheet				Conditions
			Min	Typ†	Max	Units		Min	Typ†	Max	Units	
D001	VDD	**Supply Voltage**	2.5	—	6.0	V	LP, XT, RC osc configuration (DC - 4 MHz)	2.5	—	5.5	V	A/D in use, -40°C - +85°C
								2.0	—	5.5	V	A/D not used, -40°C - +85°C
D005	BVDD	**Brown-out Reset Voltage**	3.7	4.0	4.3	V	BODEN bit in configuration word enabled	3.65	4.0	4.35	V	Same as PIC16LC76/77
D010	IDD	**Supply Current (Note 3, 4)**	—	2.0	3.8	mA	XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V, **(Note 5)**	—	0.4	2.0	mA	Same as PIC16LC76/77
D010A			—	22.5	48	mA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled	—	25	48	µA	Same as PIC16LC76/77
D015*	ΔIBOR	**Brown-out Reset Current (Note 6)**	—	350	425	µA	BOR enabled, VDD = 5.0V	—	25	200	µA	Same as PIC16LC76/77
D020	IPD	**Power-down Current (Note 4, 7)**	—	7.5	30	µA	VDD = 3.0V, WDT enabled, -40°C to +85°C	—	2.0	30	µA	Same as PIC16LC76/77
D021A			—	0.9	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C	—	0.1	5	µA	VDD = 3.0V, WDT disabled, -40°C to +85°C
D023*	ΔIBOR	**Brown-out Reset Current (Note 6)**	—	350	425	µA	BOR enabled, VDD = 5.0V	—	25	200	µA	Same as PIC16LC76/77
D130	EP	**Program FLASH Memory**										
		Endurance	N/A	N/A	N/A	N/A		100	1000	—	E/W	25°C at 5V
D131	VPR	**VDD for Read**	N/A	N/A	N/A	N/A		2.0	—	5.5	V	
D150	VOD	**Open Drain High Voltage**	—	—	14	V	RA4 pin	—	—	12	V	RA4 pin

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: For RC osc configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F76/77 be driven with external clock in RC mode.

2: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = External square wave, from-rail to-rail; all I/O pins tri-stated, pulled to VDD.
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

4: Timer1 oscillator (when enabled) adds approximately 20 µA to the specification. This value is from characterization and is for design guidance only. This is not tested.

5: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

7: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

TABLE 7: PIC16C76/77 → PIC16F76/77 EXTERNAL CLOCK TIMING REQUIREMENTS DIFFERENCES

Param No.	Sym	Characteristic	PIC16C7X Data Sheet				Conditions	PIC16F7X Data Sheet				Conditions
			Min	Typ†	Max	Units		Min	Typ†	Max	Units	
	FOSC	**External CLKI Frequency**	DC	—	4	MHz	XT and RC Osc mode	DC	—	1	MHz	XT Osc mode
			DC	—	200	kHz	LP osc mode	DC	—	32	kHz	LP Osc mode
1	TCY	**External CLKI Period**	250	—	—	ns	XT and RC Osc mode	1000	—	—	ns	XT Osc mode

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

TABLE 8: PIC16C76/77 → PIC16F76/77 CLKO AND I/O TIMING REQUIREMENTS DIFFERENCES

Param No.	Sym	Characteristic	PIC16C7X Data Sheet				Conditions	PIC16F7X Data Sheet				Conditions
			Min	Typ†	Max	Units		Min	Typ†	Max	Units	
17*	TOSH2IOV	**OSC1↑ (Q1 cycle) to Port Out Valid**	—	50	150	ns		—	100	255	ns	
20*	TIOR	**Port Output Rise Time**	—	—	80	ns	PIC16LC7X	—	—	145	ns	PIC16LF7X
21*	TIOF	**Port Output Fall Time**	—	—	80	ns	PIC16LC7X	—	—	145	ns	PIC16LF7X

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 9: PIC16C76/77 → PIC16F76/77 CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2) DIFFERENCES

Param No.	Sym	Characteristic	PIC16C7X Data Sheet				Conditions	PIC16F7X Data Sheet				Conditions
			Min	Typ†	Max	Units		Min	Typ†	Max	Units	
53*	TCCR	**CCP1 and CCP2 Output Rise Time**	—	25	45	ns	PIC16LC7X	—	25	50	ns	PIC16LF7X

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 10: PIC16C76/77 → PIC16F76/77 SPI MODE REQUIREMENTS DIFFERENCES

Param No.	Sym	Characteristic		PIC16C7X Data Sheet				Conditions	PIC16F7X Data Sheet			
				Min	Typ†	Max	Units		Min	Typ†	Max	Units
78*	TscR	**SCK Output Rise Time (Master mode)**	**PIC16LC7X**	—	10	25	ns	PIC16LF7X	—	25	50	ns
79*	TdoR	**SDO Data Output Rise Time**	**PIC16LC7X**	—	10	25	ns	PIC16LF7X	—	25	50	ns
80*	TscH2doV, TscL2doV	**SDO Data Output Valid after SCK Edge**	**PIC16LC7X**	—	—	50	ns	PIC16LF7X	—	—	145	ns

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 11: PIC16C76/77 → PIC16F76/77 A/D CONVERTER CHARACTERISTICS DIFFERENCES

Param No.	Sym	Characteristic	PIC16C7X Data Sheet				Conditions	PIC16F7X Data Sheet				Conditions
			Min	Typ†	Max	Units		Min	Typ†	Max	Units	
131	TCNV	**Conversion Time** (not including S/H time) **(Note 1)**	—	9.5	—	TAD		9	—	9	TAD	
A20	VREF	**Reference Voltage**	3.0	—	VDD + 0.3	V		2.5	—	VDD + 0.3	V	-40°C to +125°C
								2.2	—	VDD + 0.3	V	0°C to +125°C
A50	IREF	**VREF Input Current (Note 1)**	10	—	1000	µA	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see device data sheet.	N/A	—	±5	µA	During VAIN acquisition.
			—	—	10	µA	During A/D Conversion cycle.	—	—	500	µA	During A/D Conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products.

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Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.

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